Overview of the Global Trigger and Synchronization System

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Rates

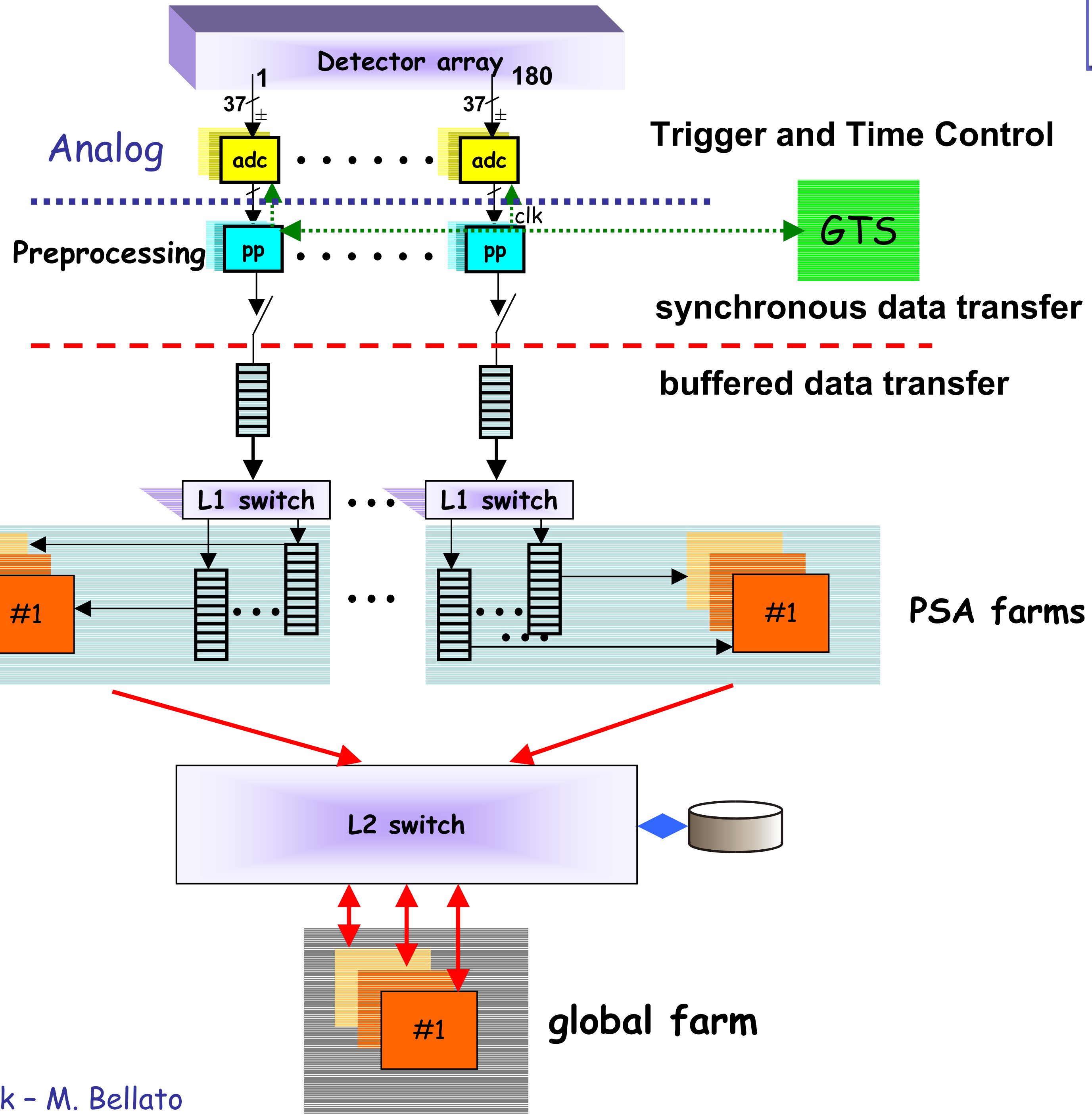
200 MB/s/seg
7.4 GB/s/det

100 MB/s/det

5 MB/s/det

900 MB/s

100 MB/s



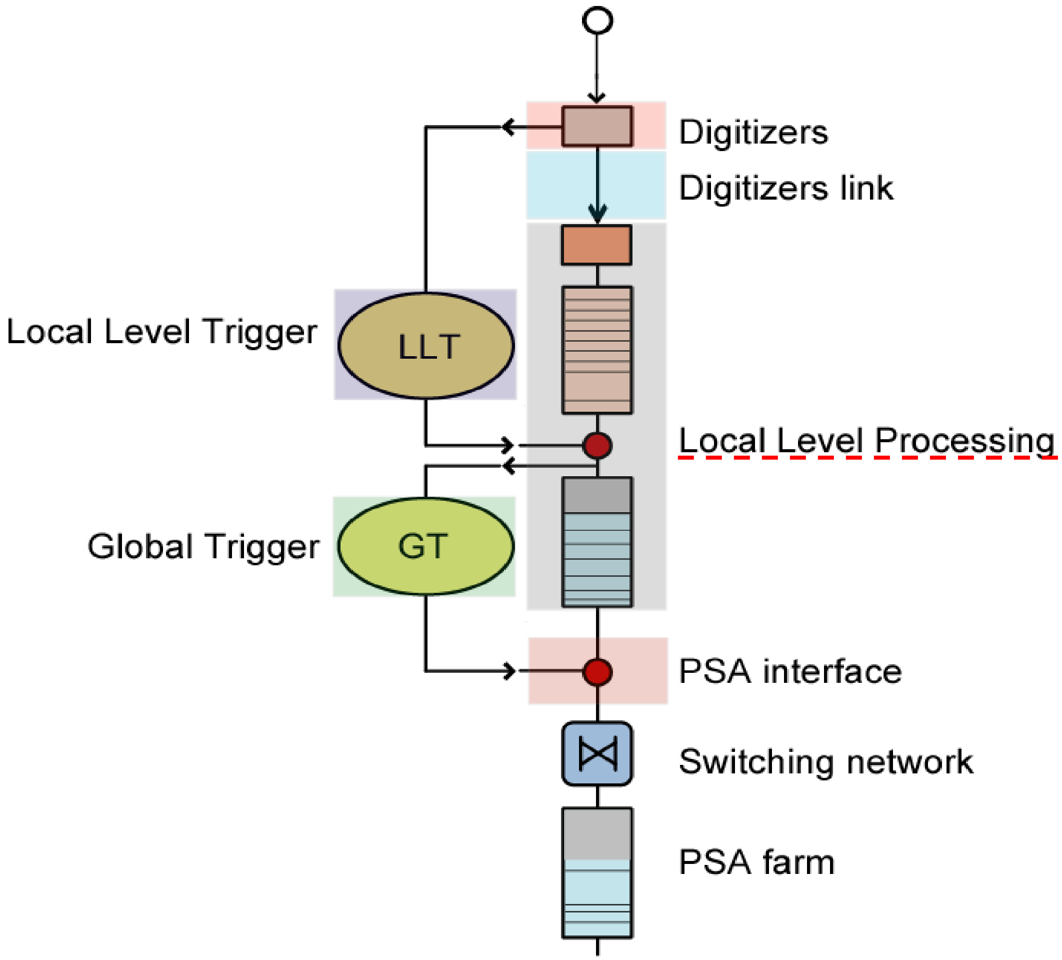
Introduction

- AGATA is essentially a triggerless system
- Information stored in the leading edge of pulses
  - Need of a global time reference for all samplers
- A trigger is built locally by data processing
  - Much like a digital scope system "smart trigger"
  - Zero suppression without loss of information at the front-end level
  - ADC sample granularity
  - Source of dead time
- A global trigger is built on local triggers, provided a suitable infrastructure
  - Data reduction by event selection (with loss of information)
  - Source of latency

Requirements of GTS

- Global time reference (100 MHz)
- Global trigger processing and distribution
- Time-referenced command distribution (unicast, multicast and broadcast)
- Synchronous custom logic triggering (e.g. periodic calibration pulse generation in FADC logic)
- Trigger partitioning into independent sub-systems
- Trigger logic customization

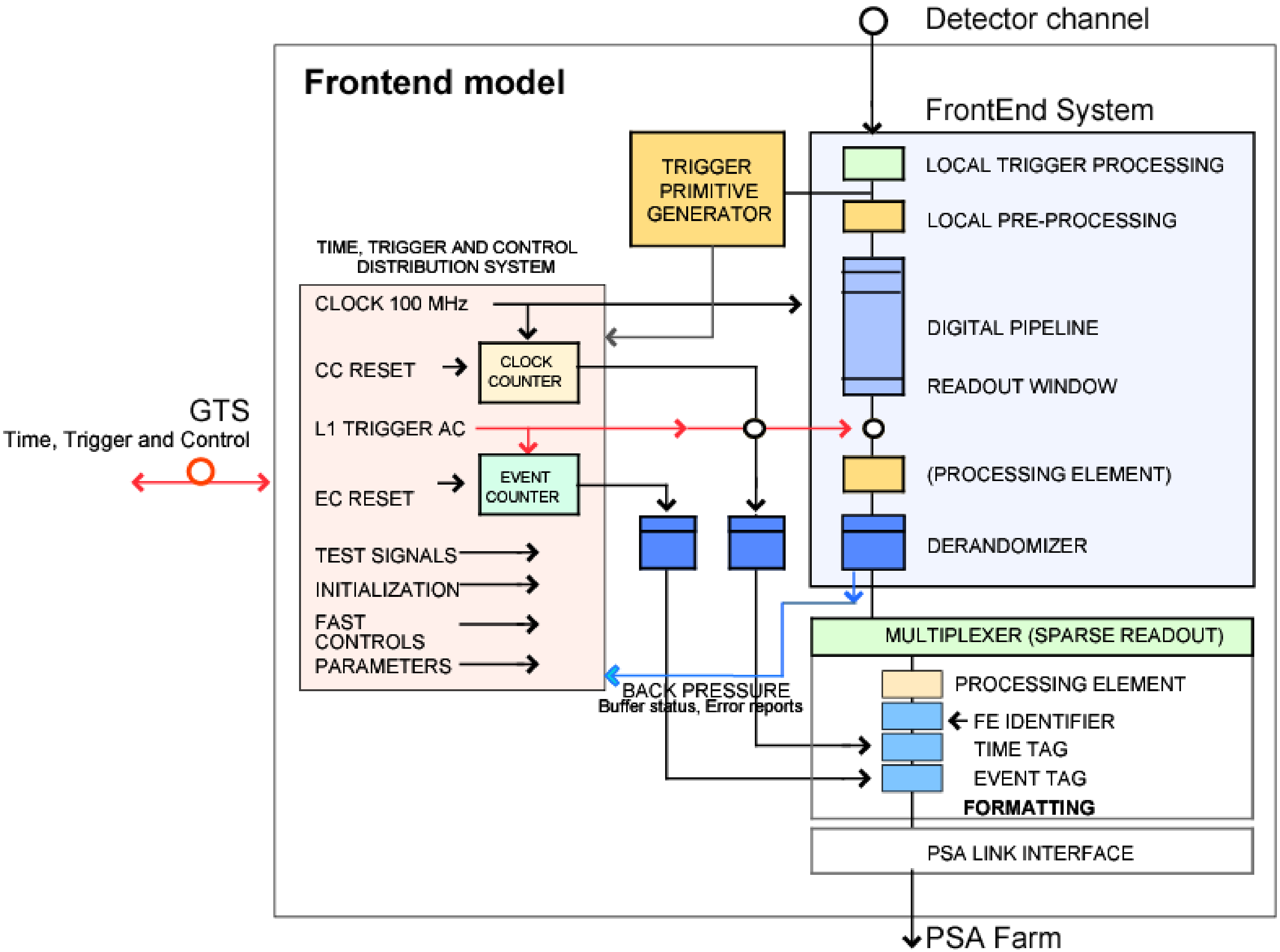
Model of the GTS functionality-1



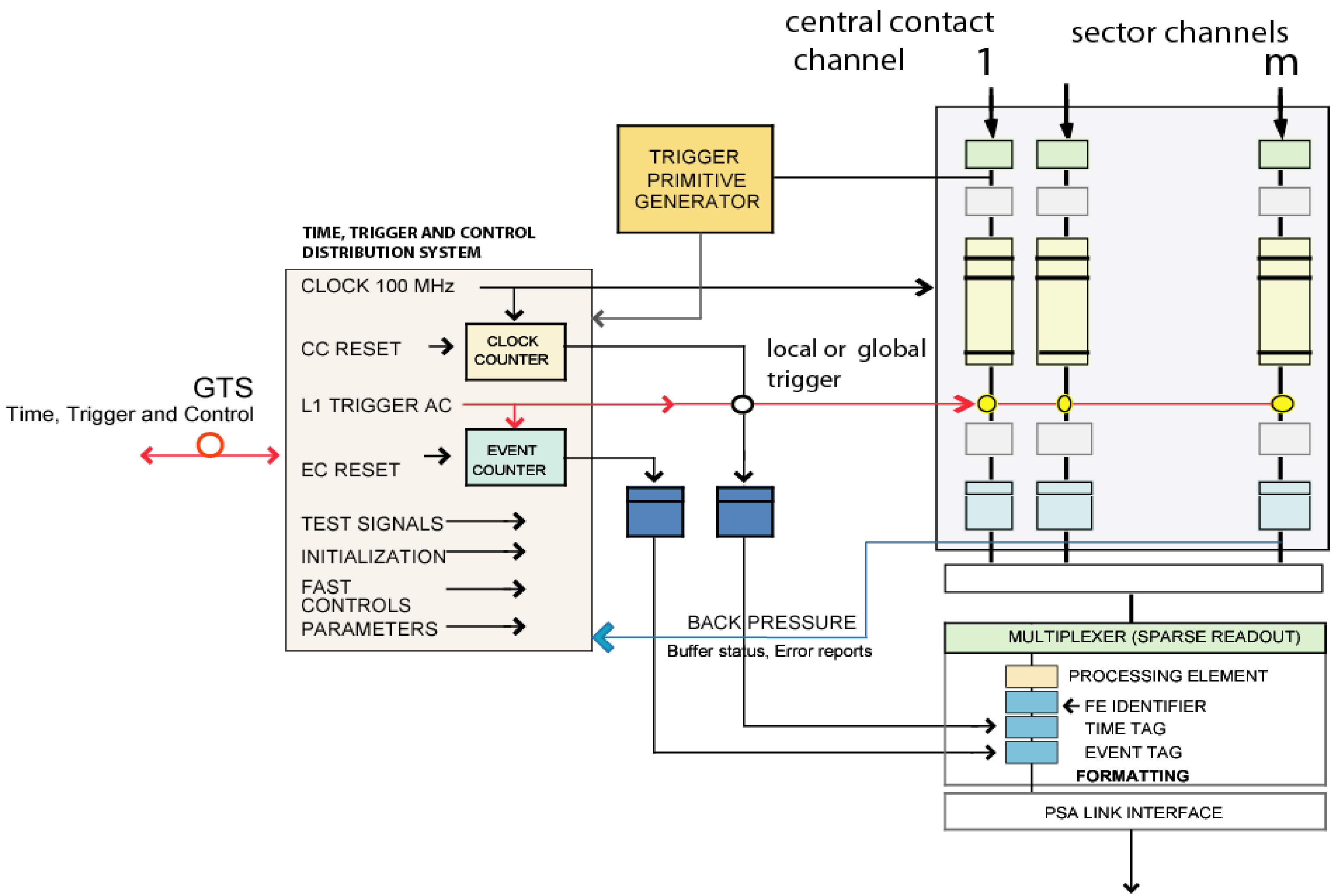
global clock
synchronous domain

buffered domain

Model of the GTS functionality-2



Model of the GTS functionality-3



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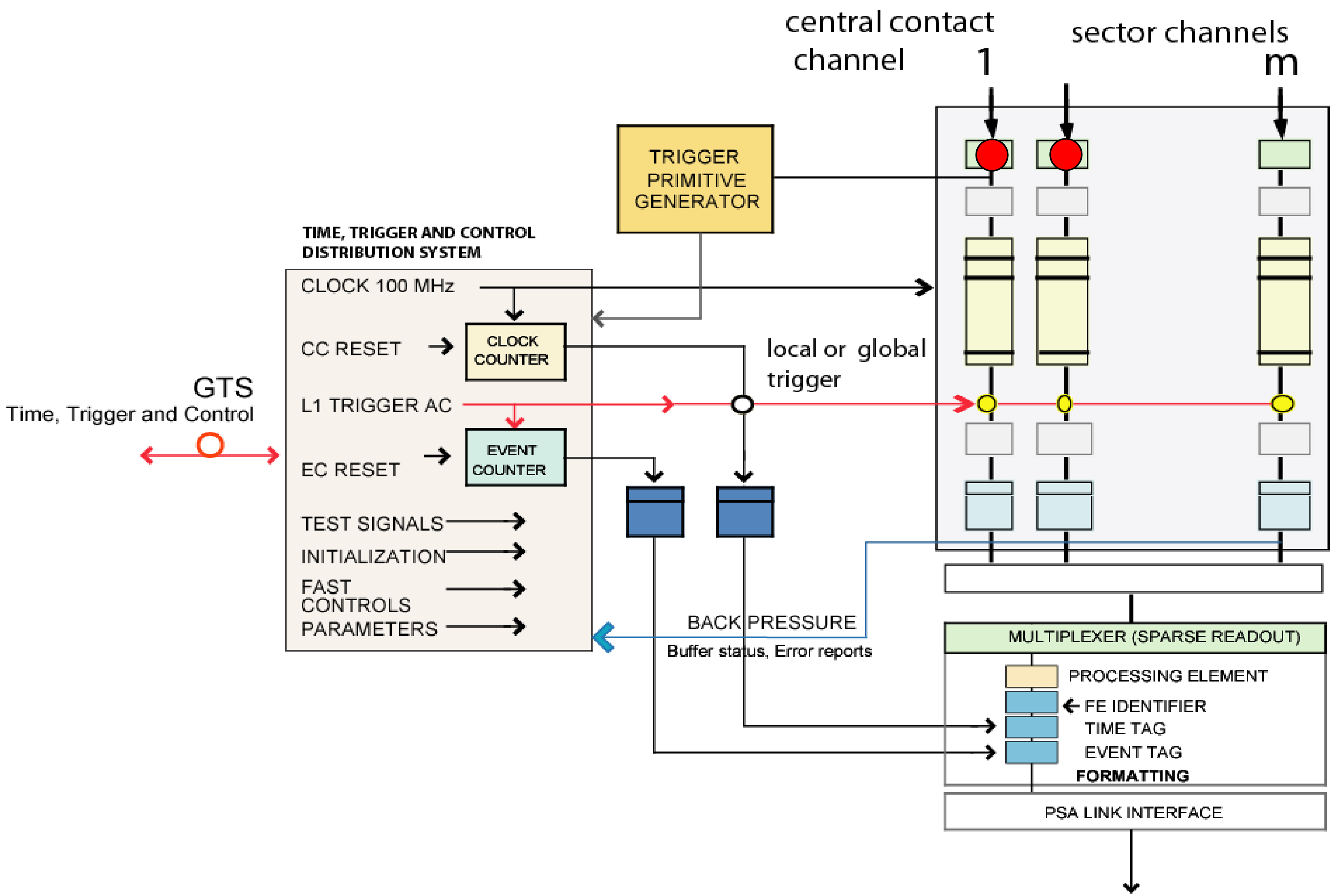

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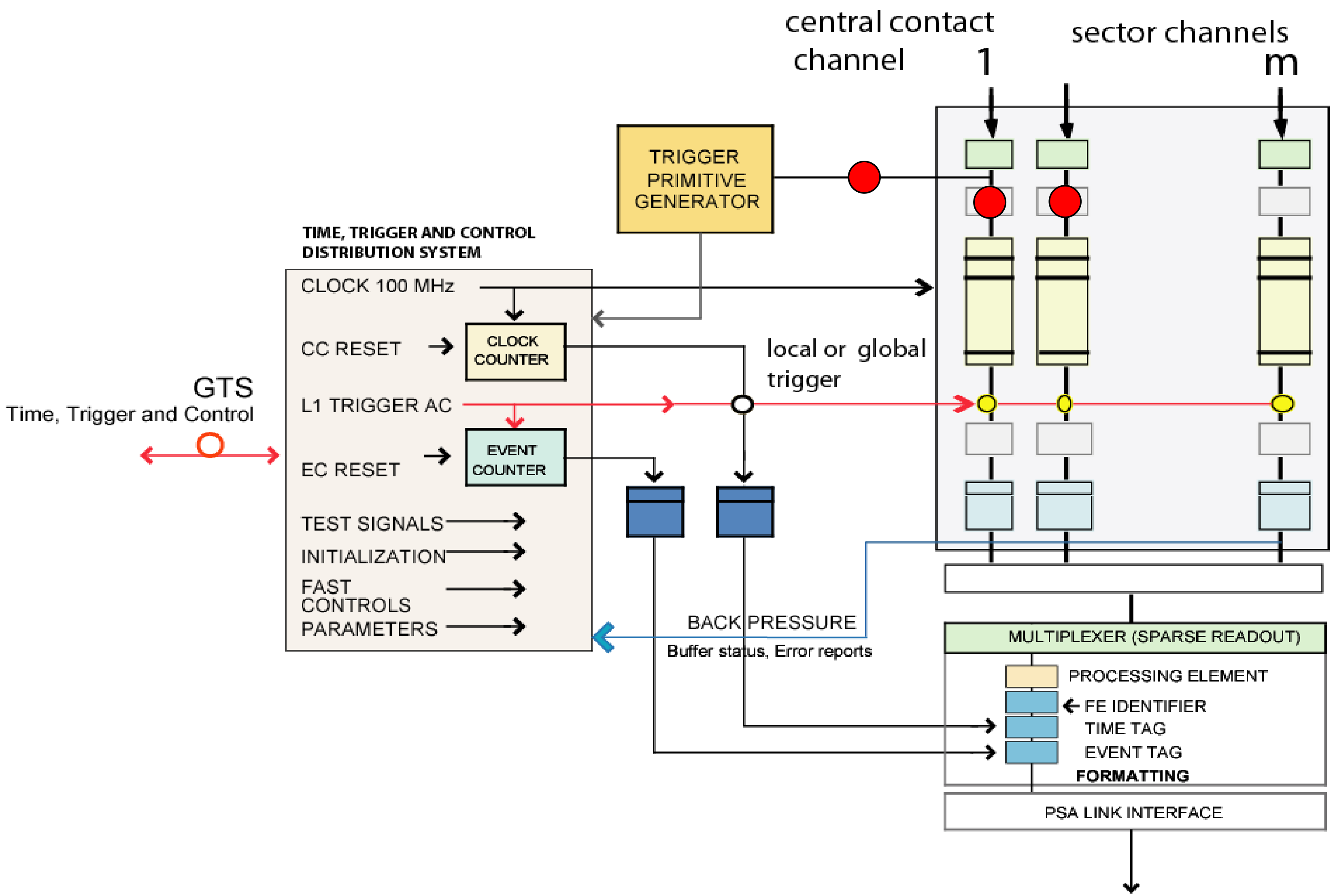

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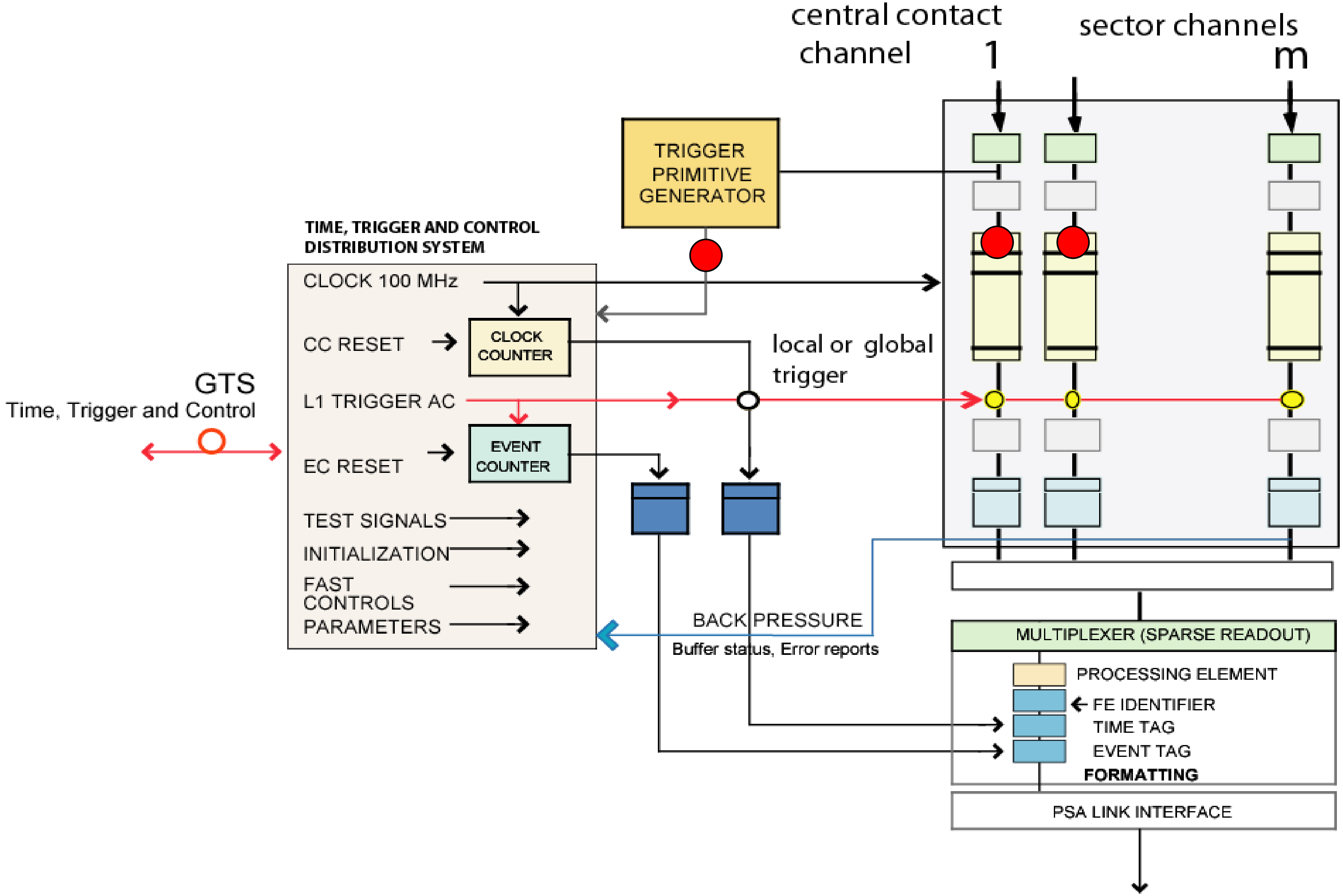

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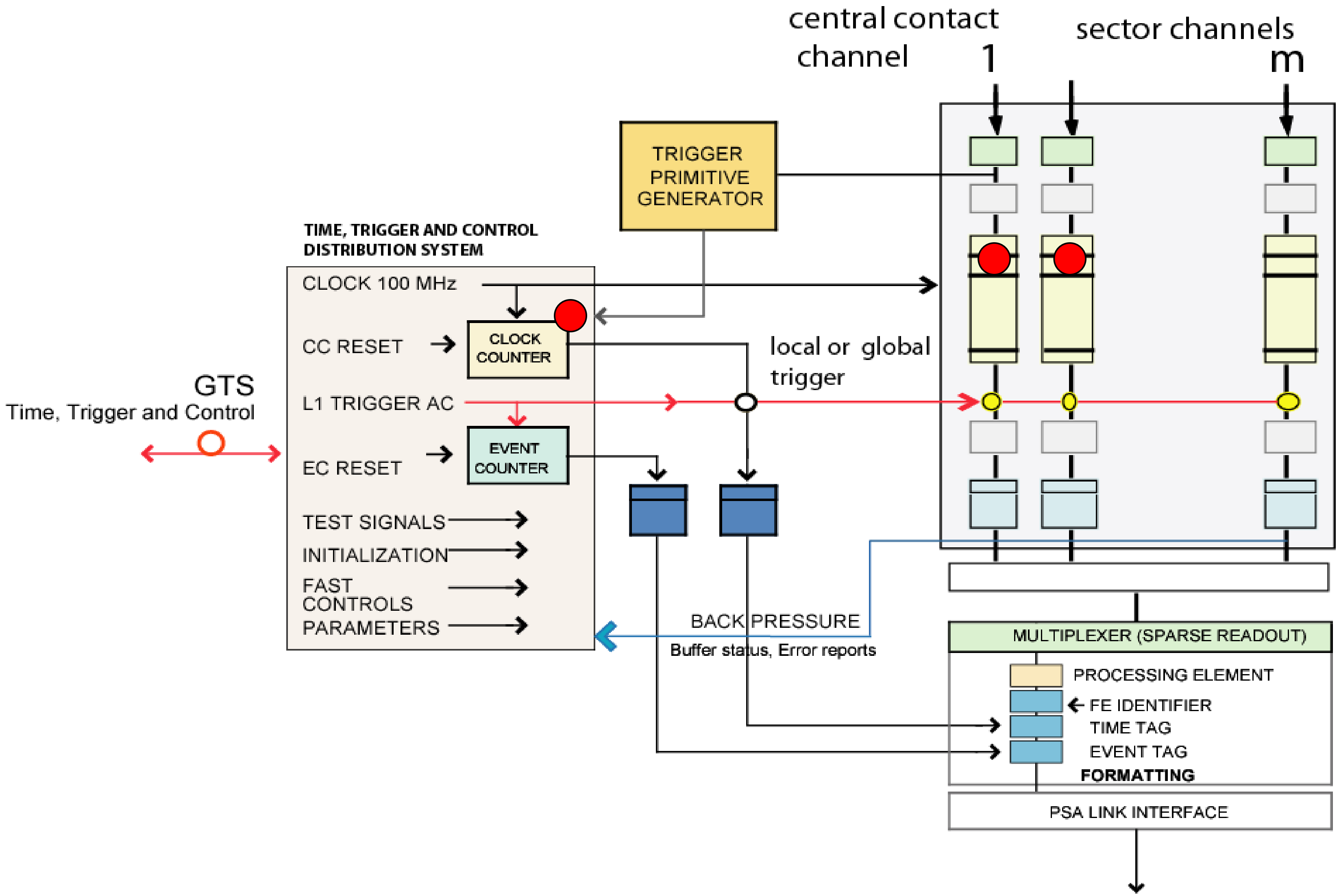

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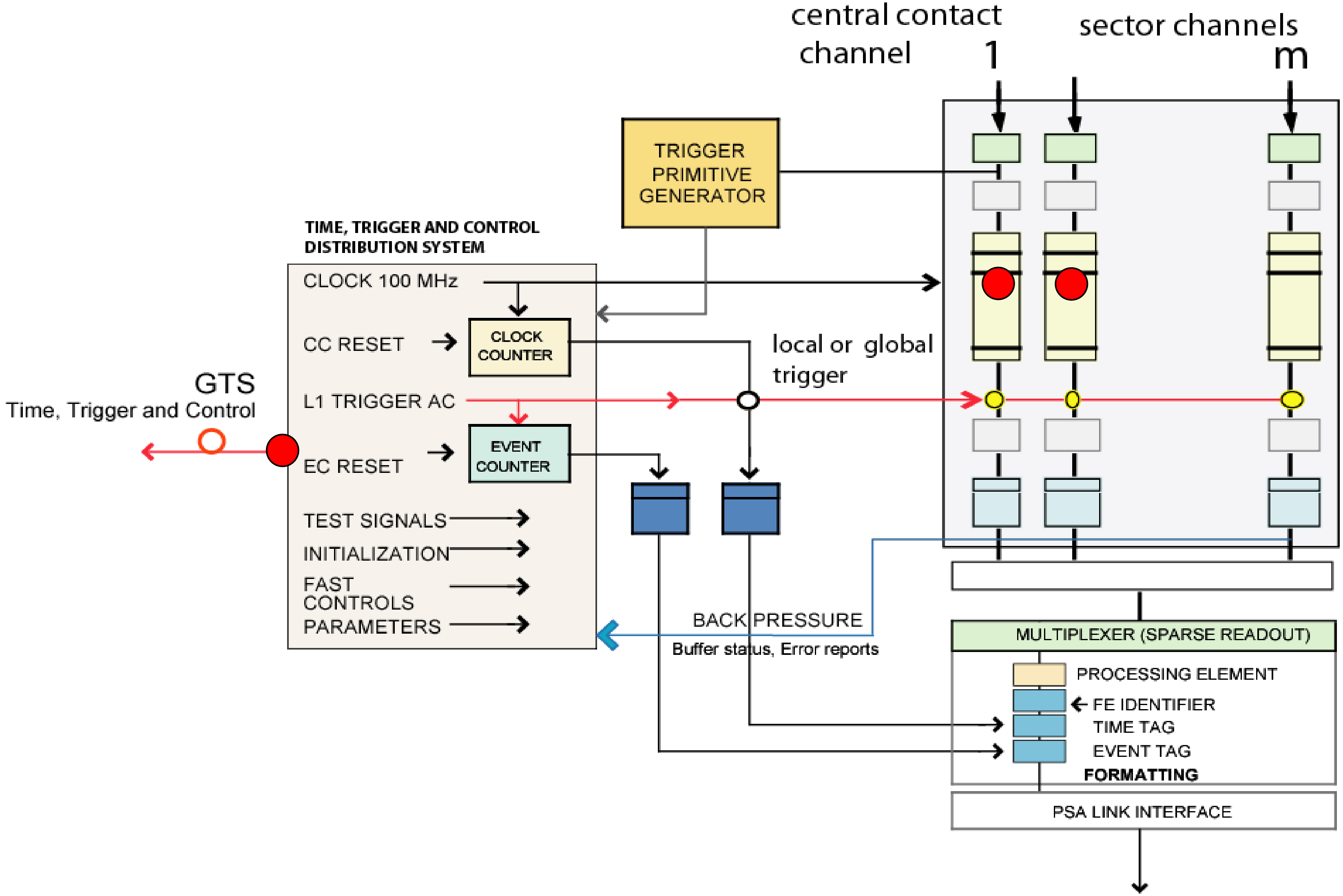

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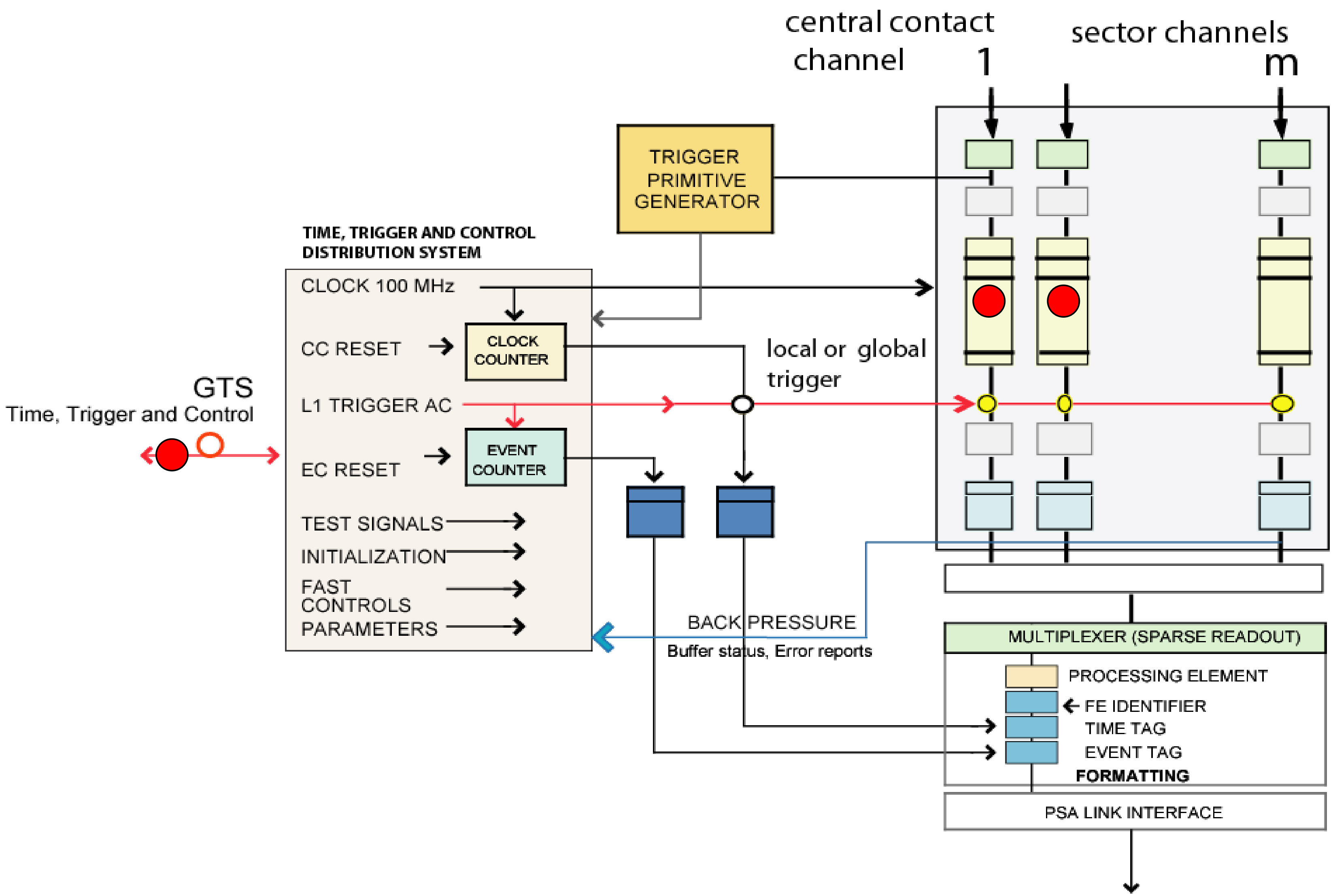

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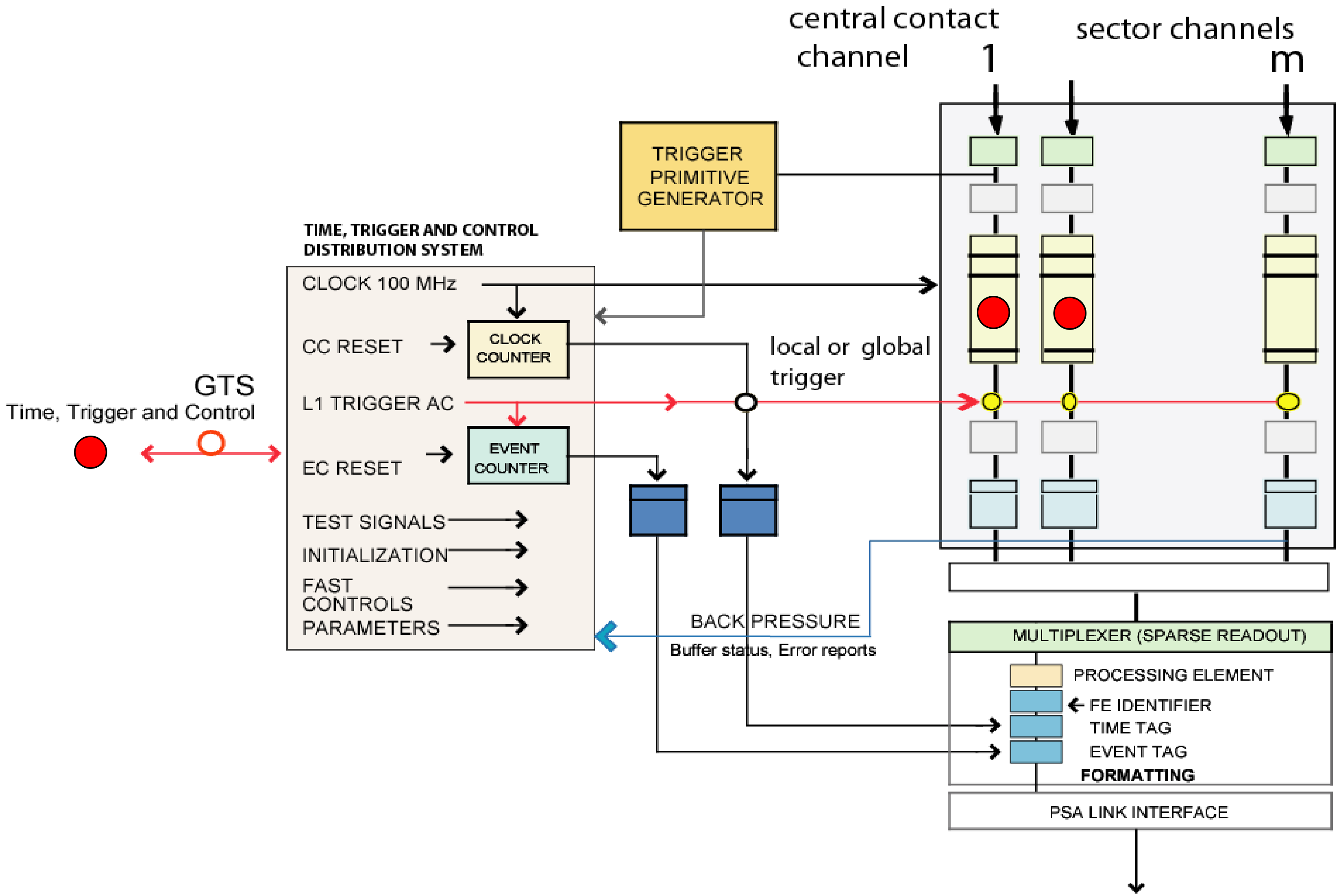

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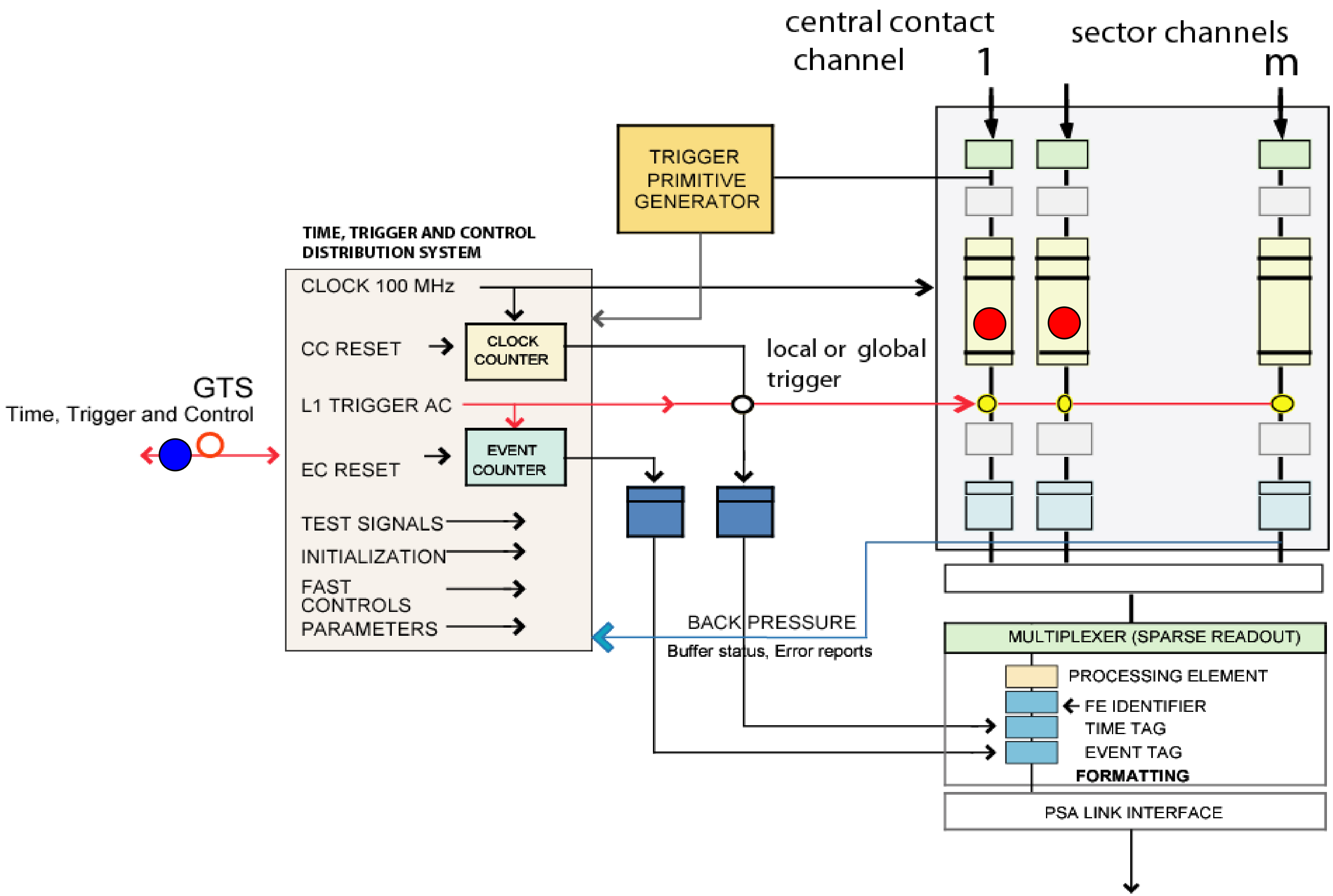

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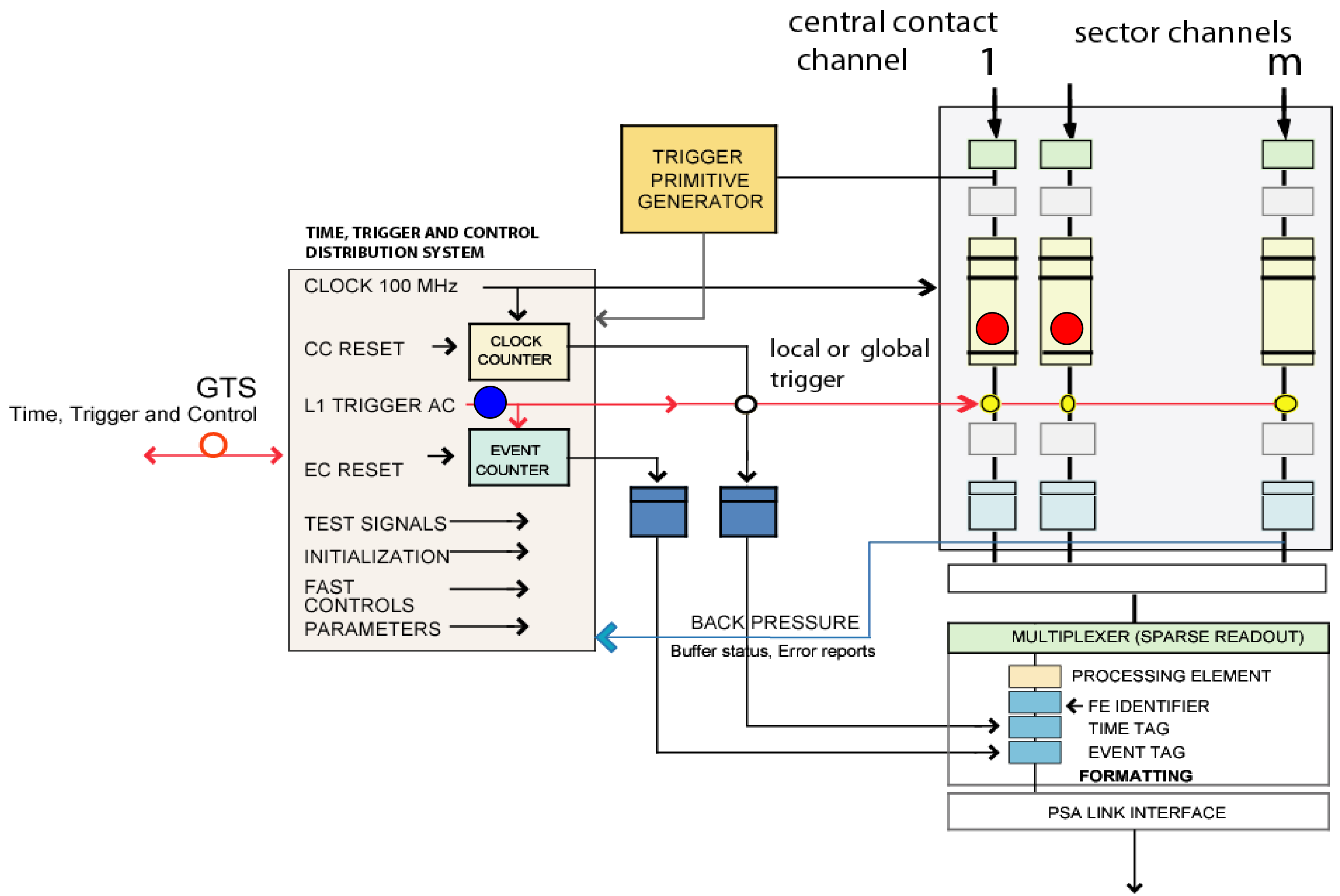

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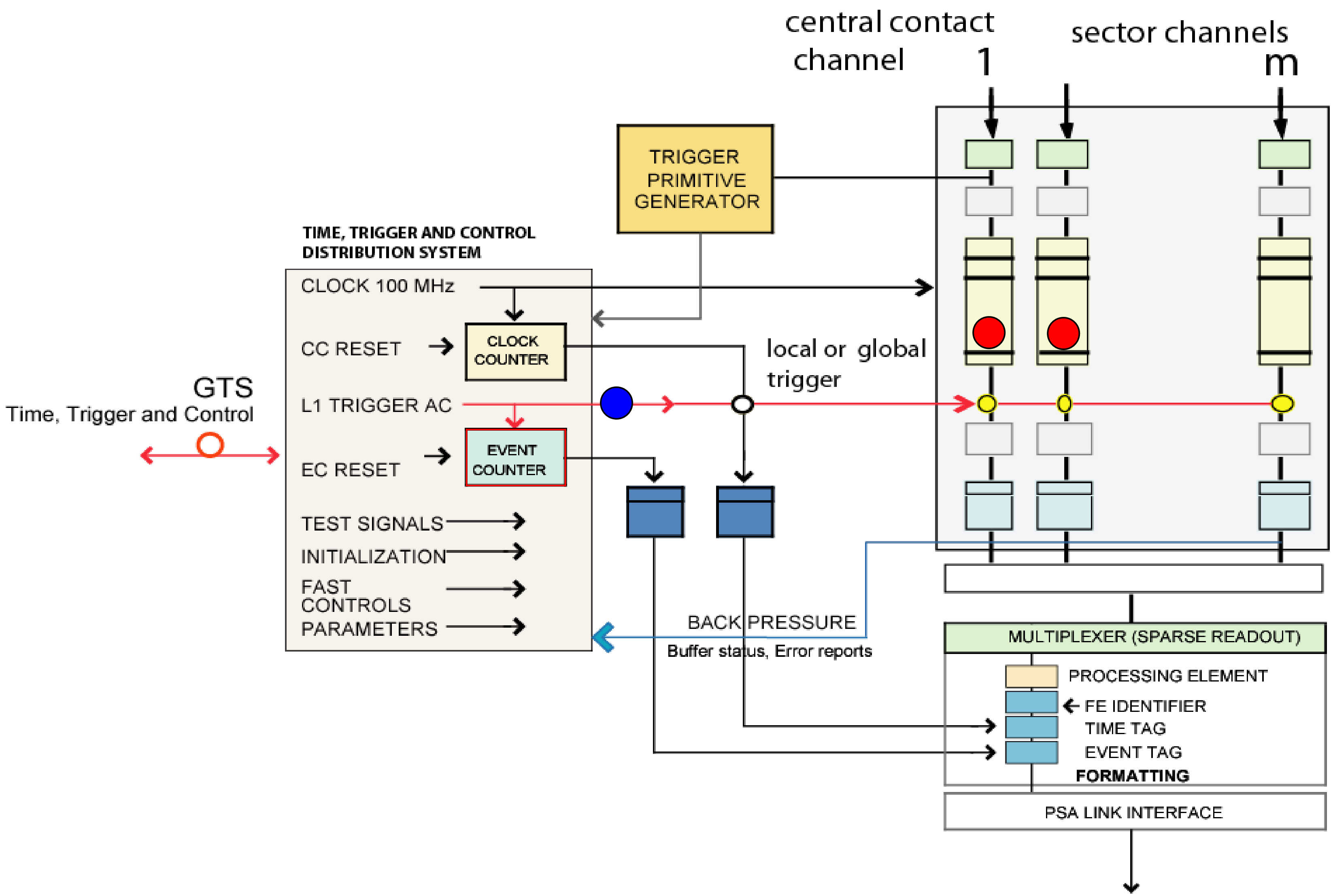

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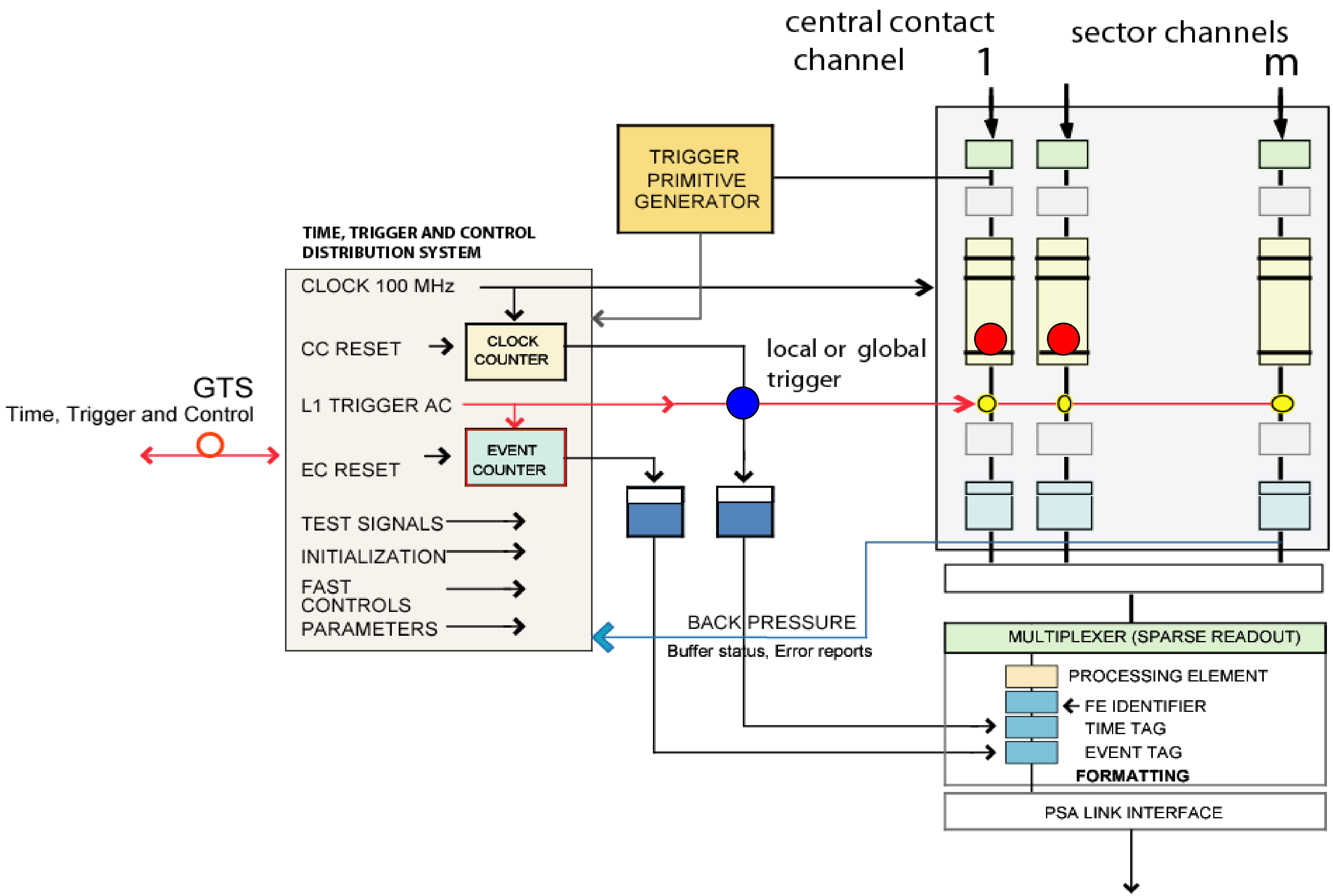

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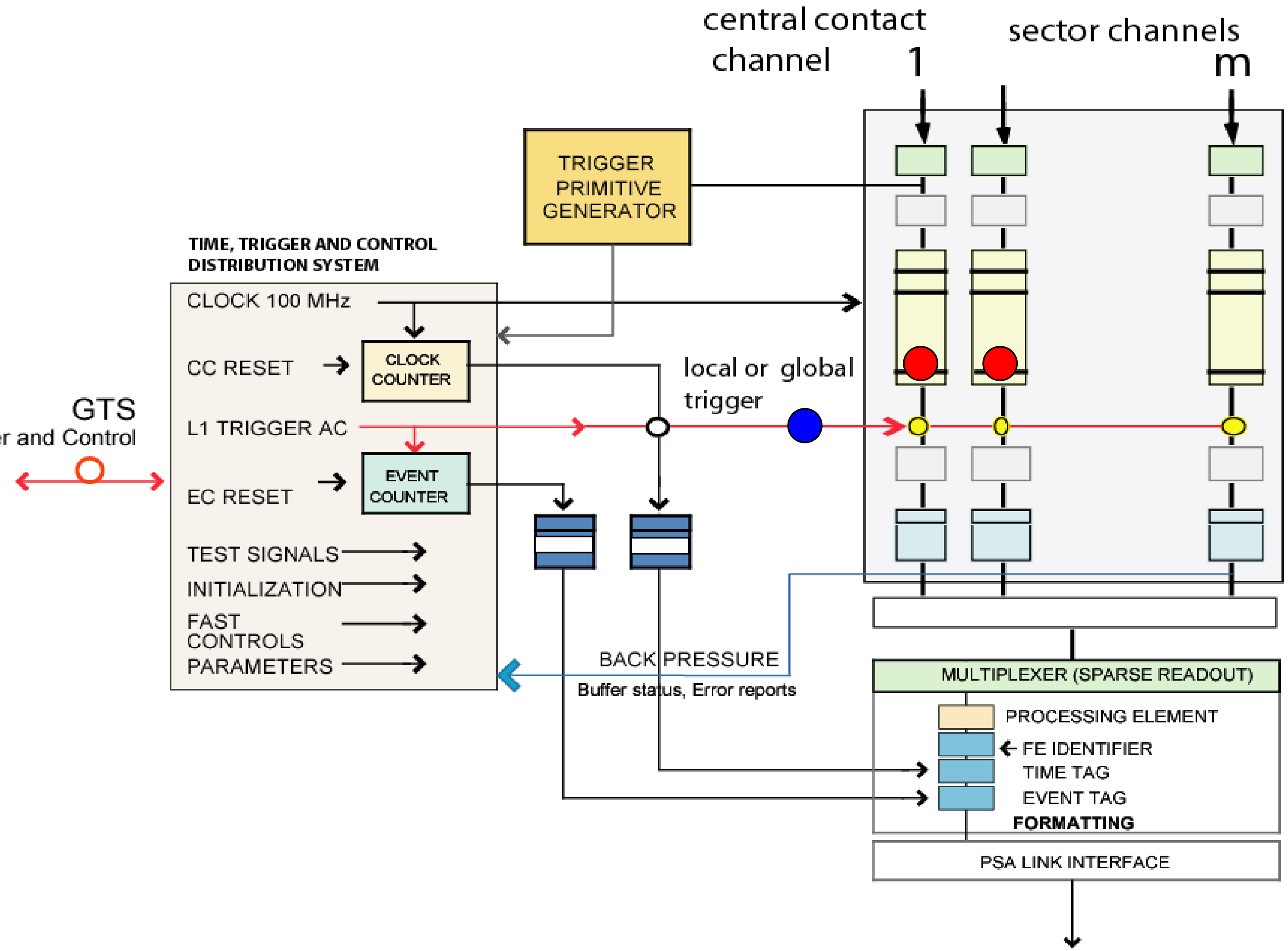

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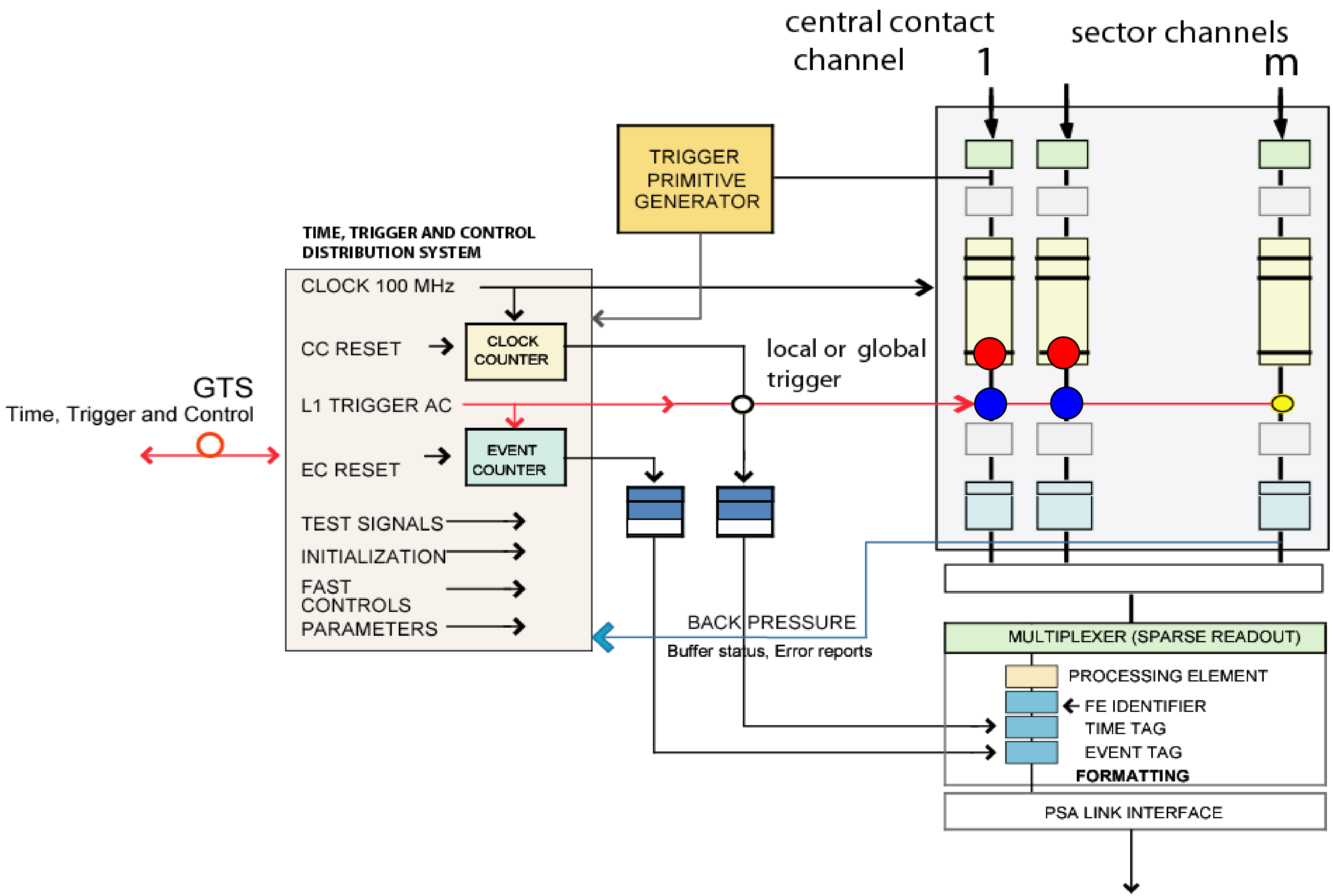

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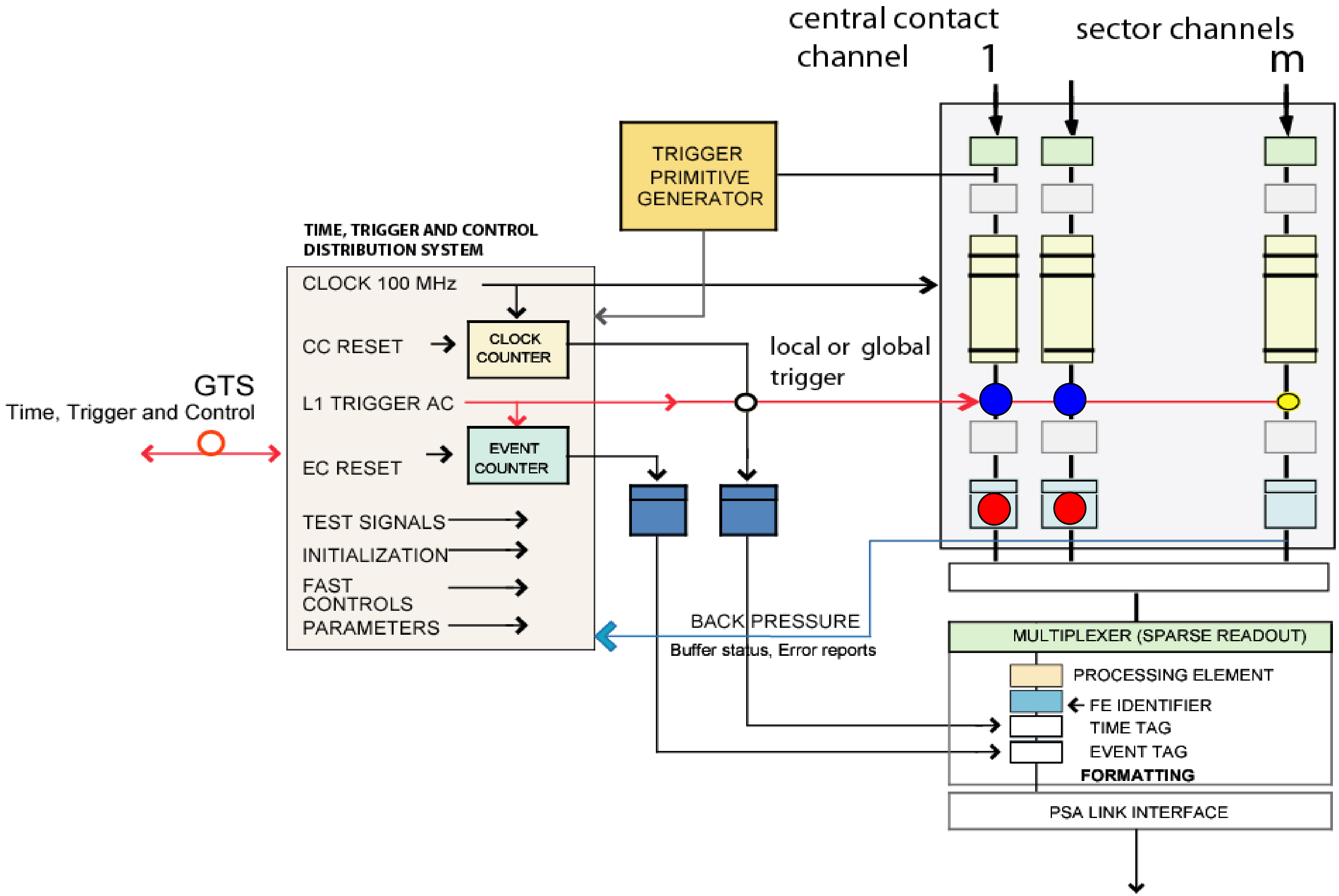

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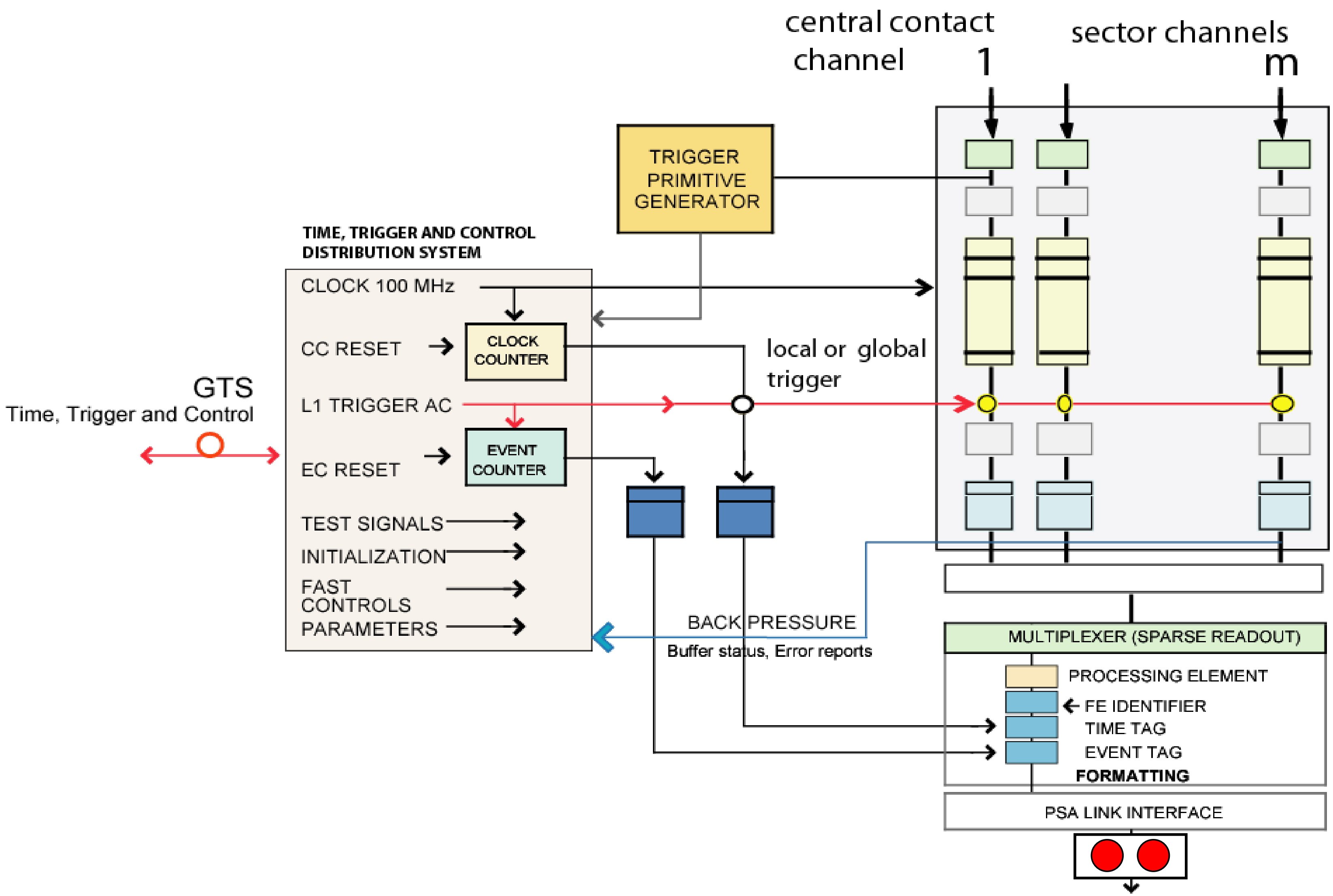
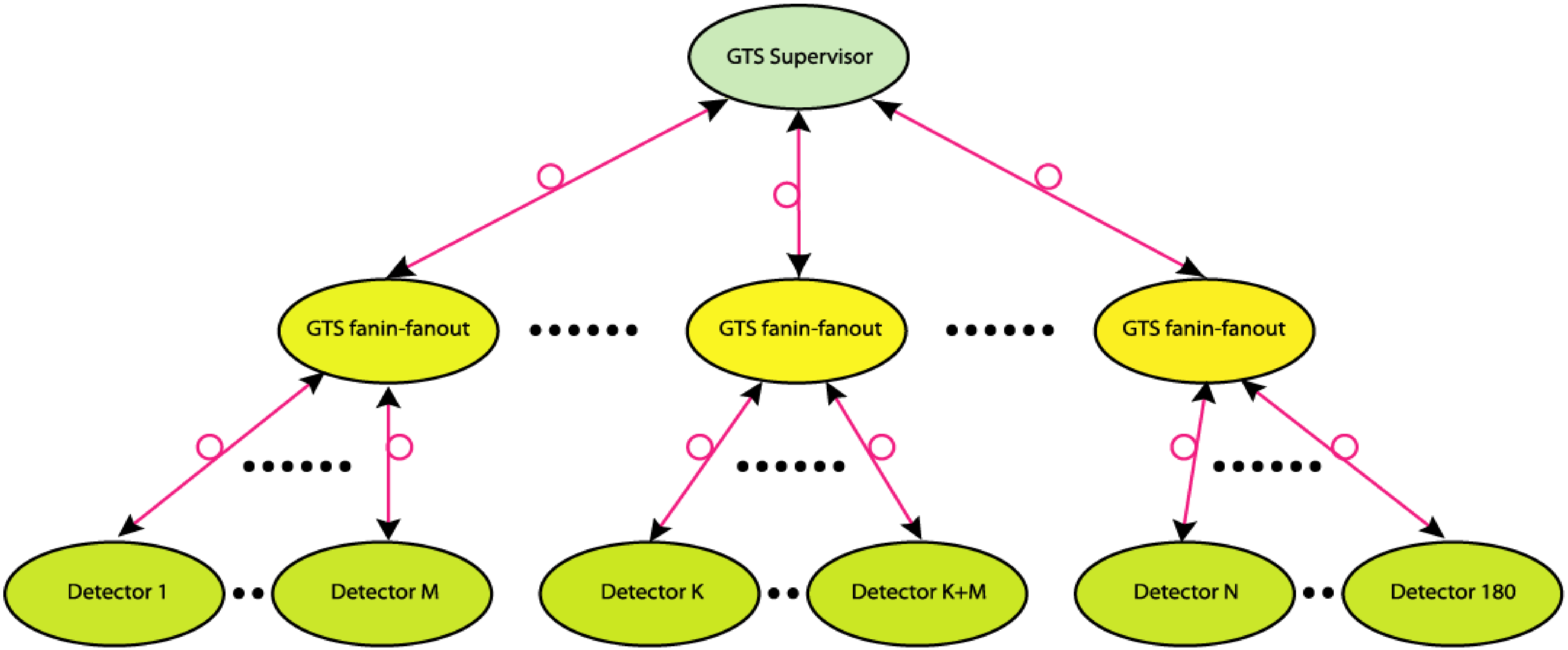


Tree-structure approach for GTS -1



Tree-structure approach for GTS -2

- Tree can be balanced for phase alignement at the end nodes
- Root node is the single point of data broadcasting
- Fanin-fanout nodes may act as root nodes in GTS sub-trees
- Root node acts as central trigger processor and command initiator
- Global clock and global trigger functionalities can be merged together
- Trigger requests from detectors can be sent to root node at each global clock cycle
- Each detector is geographically addressable by the root node and viceversa
- Trigger validations are sent from root node to detectors after a suitable processing time (e.g. length of the matching time window for a simple multiplicity algorithm)

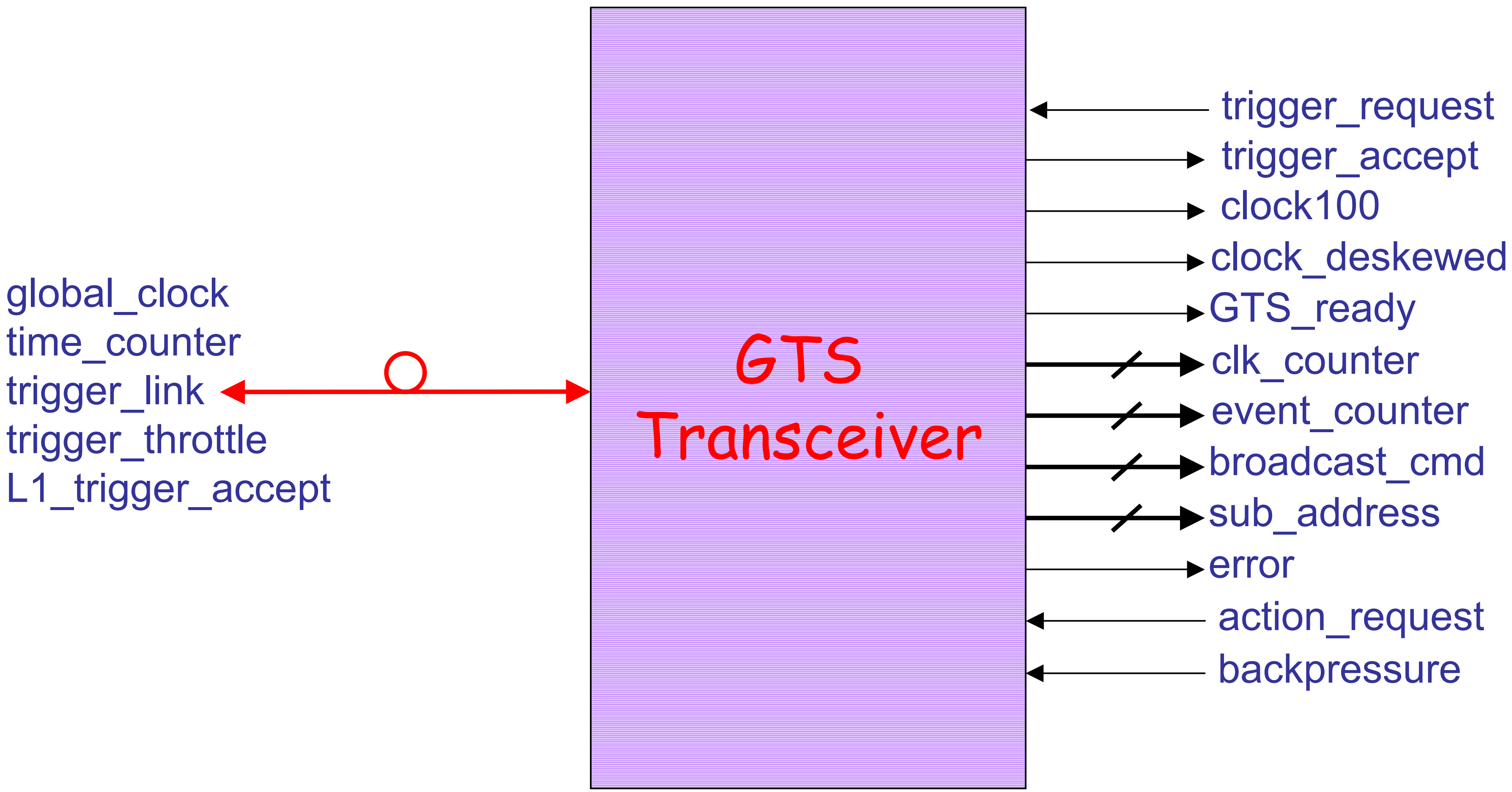
GTS Supervisor

- Distributes:
  - Global clock @ 100MHz
  - Time counter 48bit
  - Event Counter
  - Trigger validations
  - Global commands
- Receives:
  - Trigger requests – 2bit per detector per clock cycle
    - Potentially handles 180 trigger requests every 10ns
  - Action requests (e.g. Trigger throttle)

GTS Fanin-Fanout

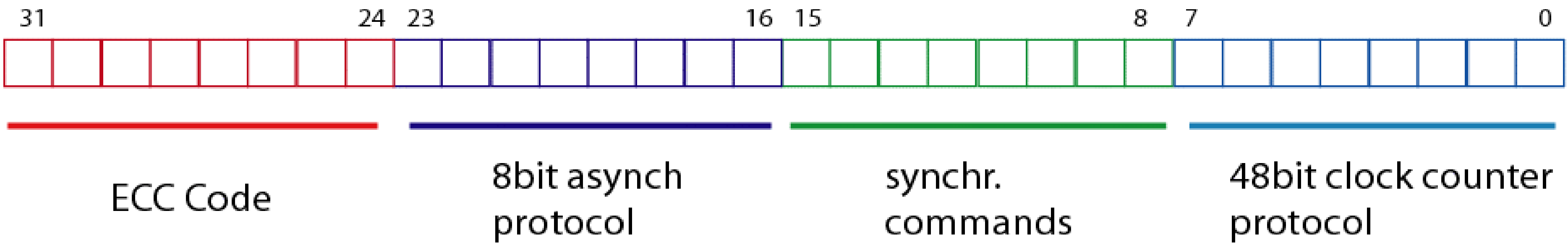
- Receives:
  - Supervisor broadcast from root node
  - Trigger requests from crystals
- Distributes:
  - Supervisor broadcast to 16 crystals
  - Merged trigger requests to supervisor
- Implements:
  - Multicast tables for selective broadcast
  - Clock equalization procedures
  - Alignment checks

GTS Mezzanine



GTS Protocol

- Electrical and optical lines implement a 32 bit bidir. datapath @ 100 MHz between each two nodes of the tree



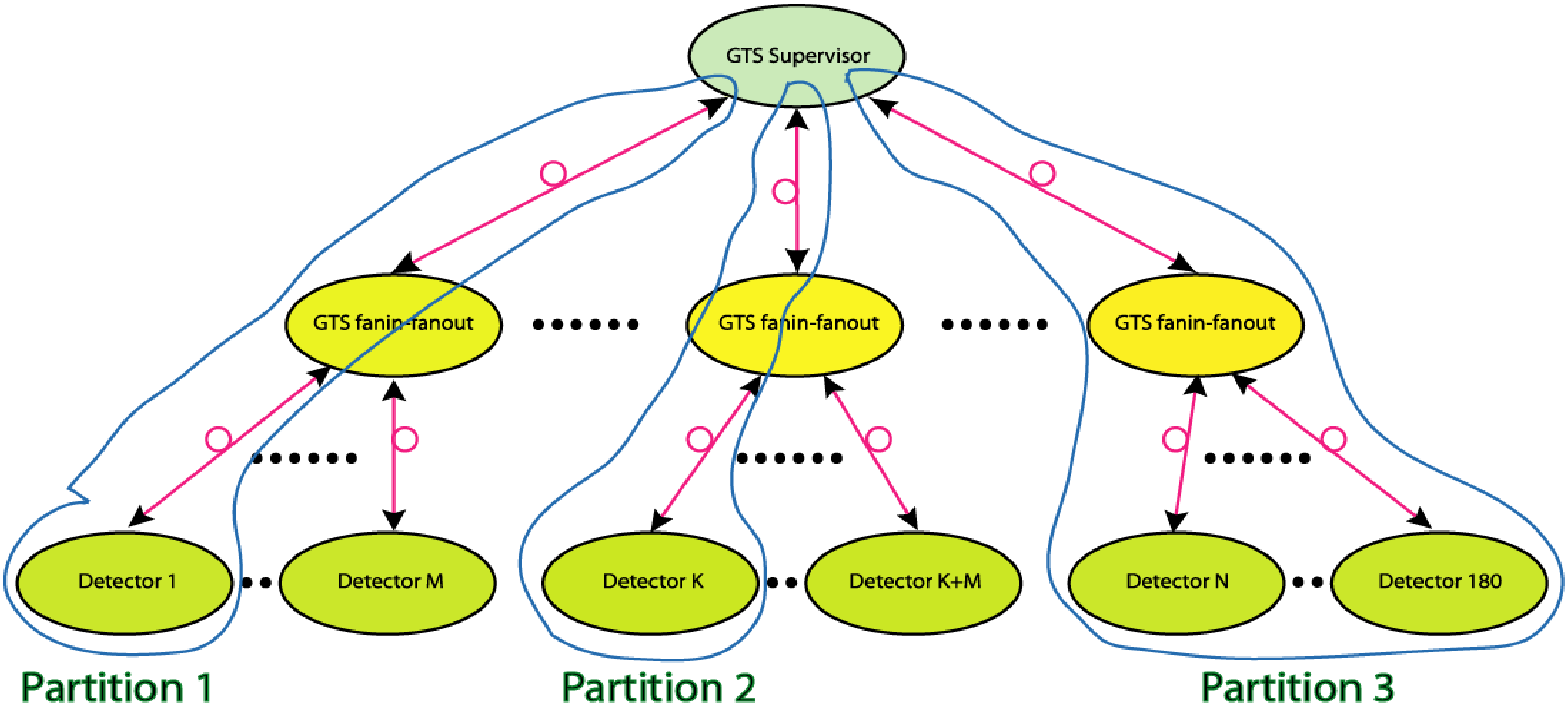
Front-end system Dead Time

- r = trigger rate
- d = dead time
- P = probability of at least one trigger occuring during dead time =

$$
\begin{aligned}
P &= 1-\left(e^{-rd}\times\frac{(rd)^0}{0!}\right)\\
&= 1-e^{-rd}\\
&\approx rd
\end{aligned}
$$

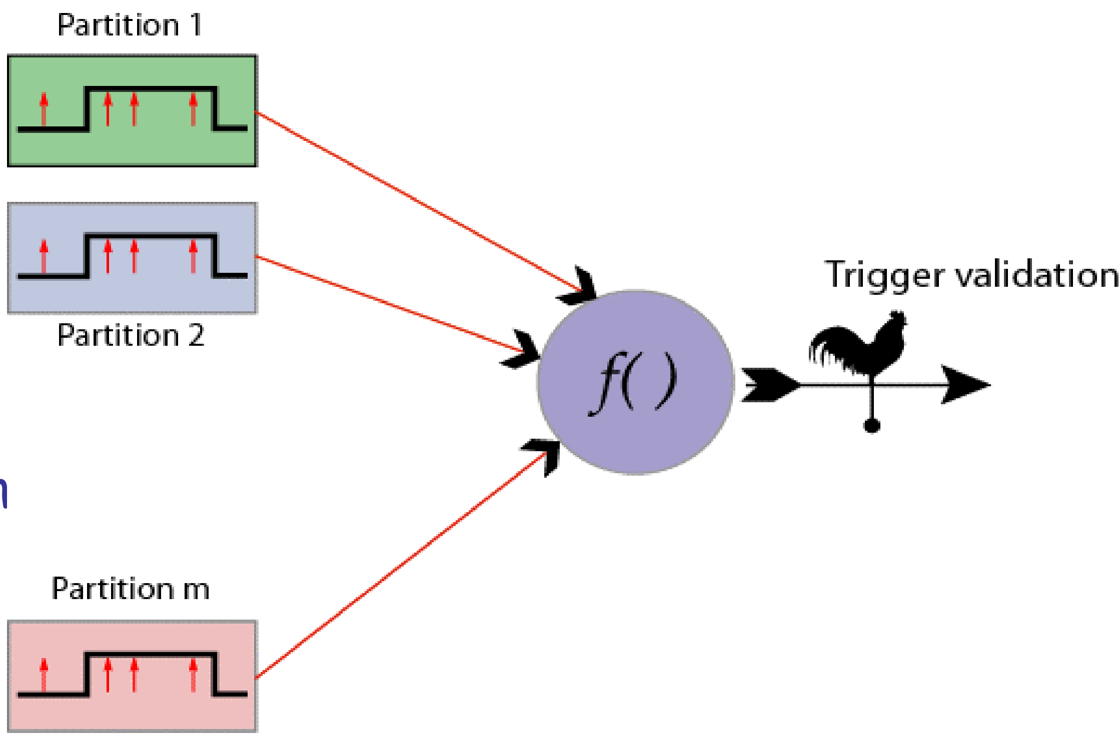
At 50KHz central contact trigger rate we lose 1% efficiency every 20 clock cycles of dead time

Trigger Partitions/1

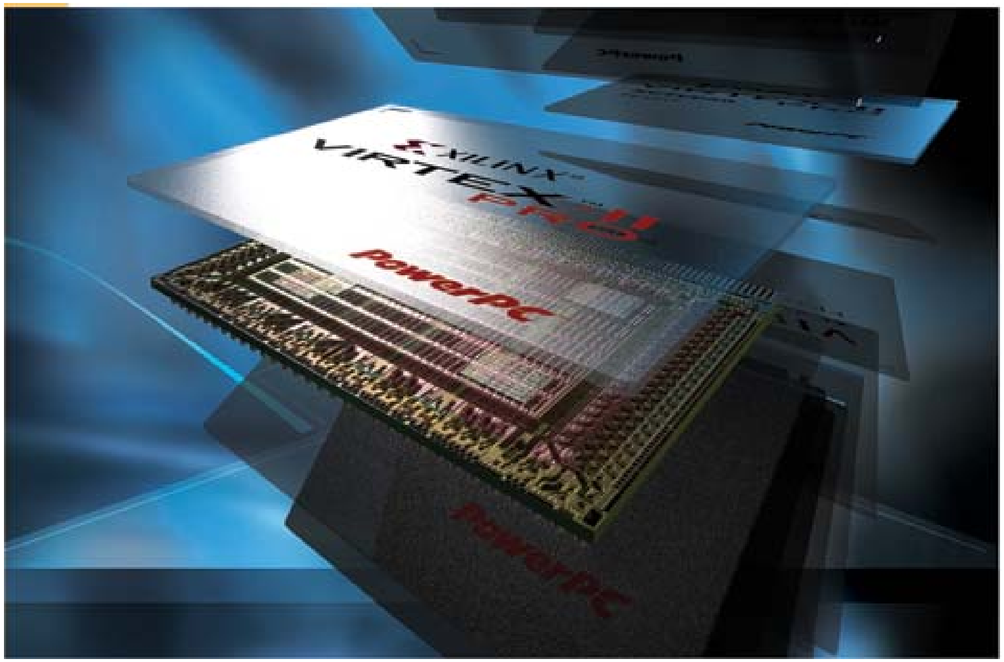


Trigger Partitions/2

- The whole trigger system seen as a union of non overlapping subsets
- Each crystal knows to which partition it belongs
- Ancillary detectors can be seen as independent partitions
- The trigger function is the result of a boolean operation on partitions
- Partitions implemented by means of a multicast mechanism

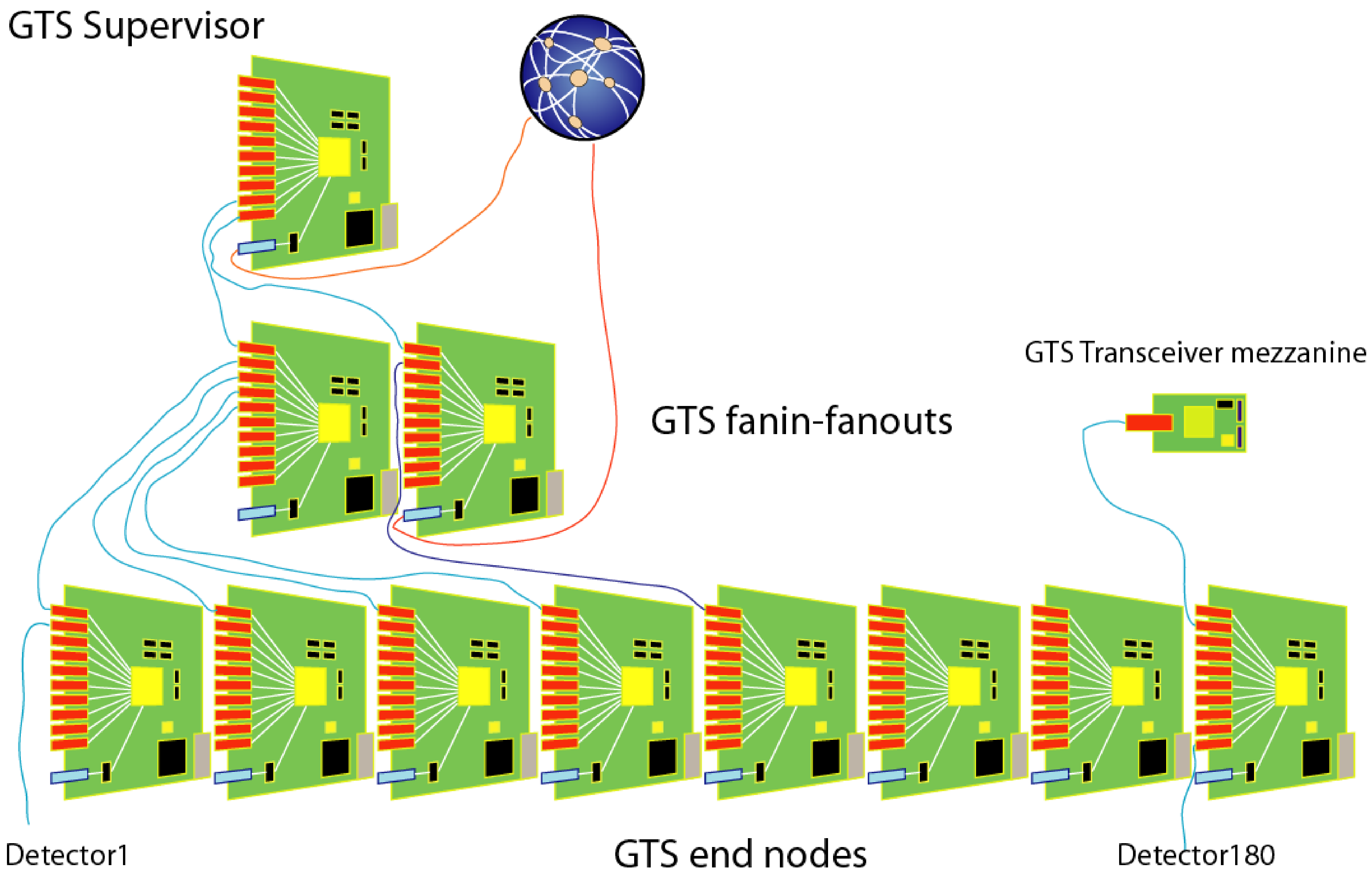


Technology highlight

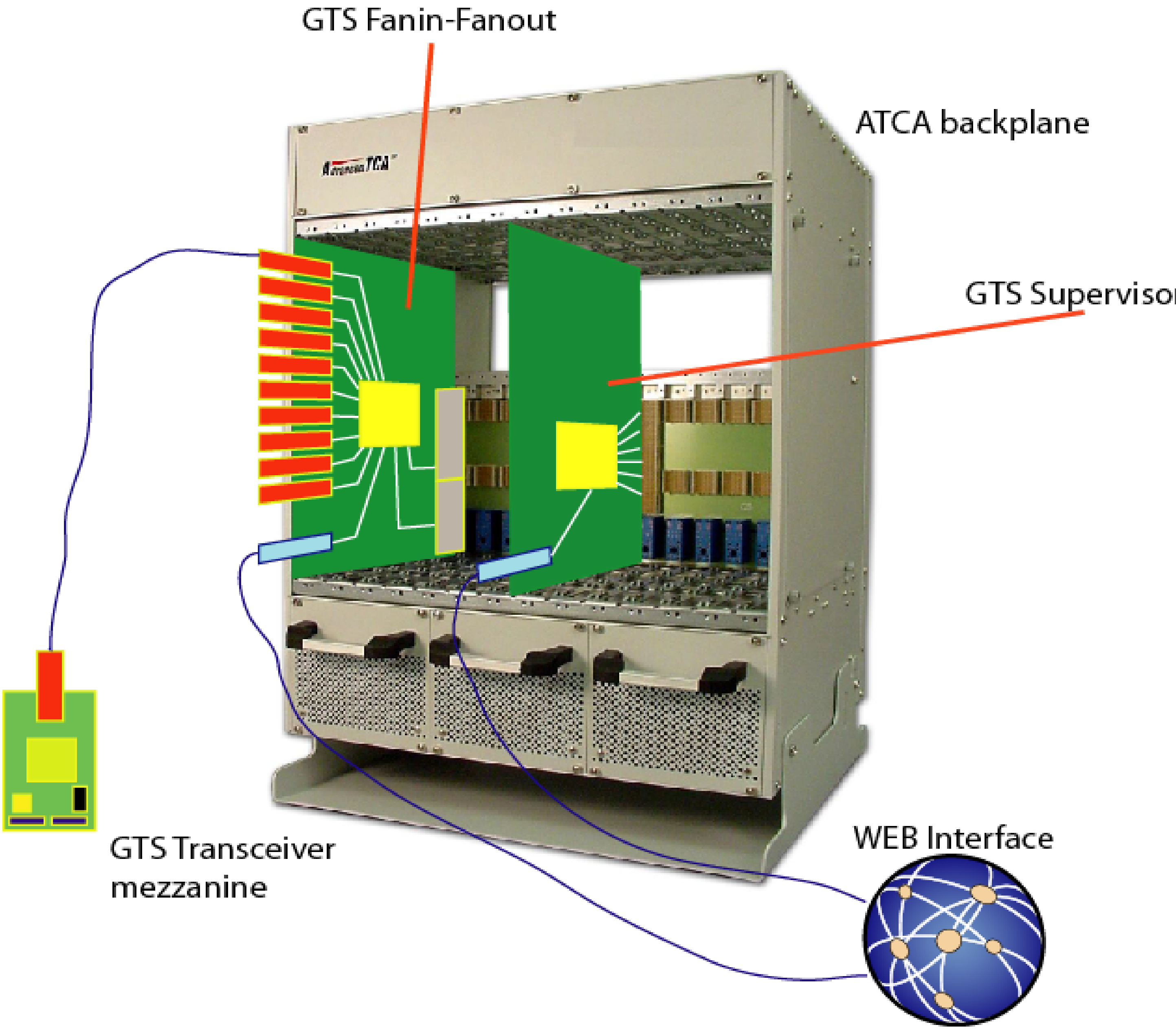


- Serial bidir transceivers embedded in FPGA core + a PowerPC CPU allows
    - Sourcing 100MHz global clock with a 32bit word
    - Receiving trigger requests at each clock cycle
    - Having million of gates of custom logic
    - Running a standard OS + a WWW server for control, calibration, testing,…
    - Reconfiguring online for maintenance

Implementation Overview 1



Implementation Overview 2



To be done...

- Central Supervisor
  - Pcb 1.5 y/man (2 cycles)
  - Fpga programming 1 y/man
- Fanin-fanout
  - Pcb 1.5 y/man (2 cycles)
  - Fpga programming 9m/man
- GTS mezzanine
  - Pcb 1 y/man (2 cycles)
  - Fpga programming 1 y/man
- Simulations 1 y/man

Total estimated 7.9 y/man

Cost Estimate

- Atca crate ~ 10Keuro
- Optical Transceivers ~ 20Keuro
- Fpga's ~ 16Keuro
- PCB's ~ 20Keuro
- PLL's ~ 2.4Keuro
- Connectors ~ 2.5Keuro
- NRE costs ~ 20Keuro

Total ~ 91Keuro

A detailed estimate can be done in a short time

Conclusions

- A global clock, trigger and control facility can be built by exploiting high speed serial bidirectional links and custom logic
- This approach avoids the need for separate global clock and trigger networks and distributed counters
- The structure is hierarchical and can be partioned
- Logical operations allowed on trigger partitions
- By adopting a lightweight protocol, commands and controls can be routed to single detectors
- Trigger requests possible at each clock cycle, trigger validations depend on validation algorithm
- Global trigger latency in the order of few us