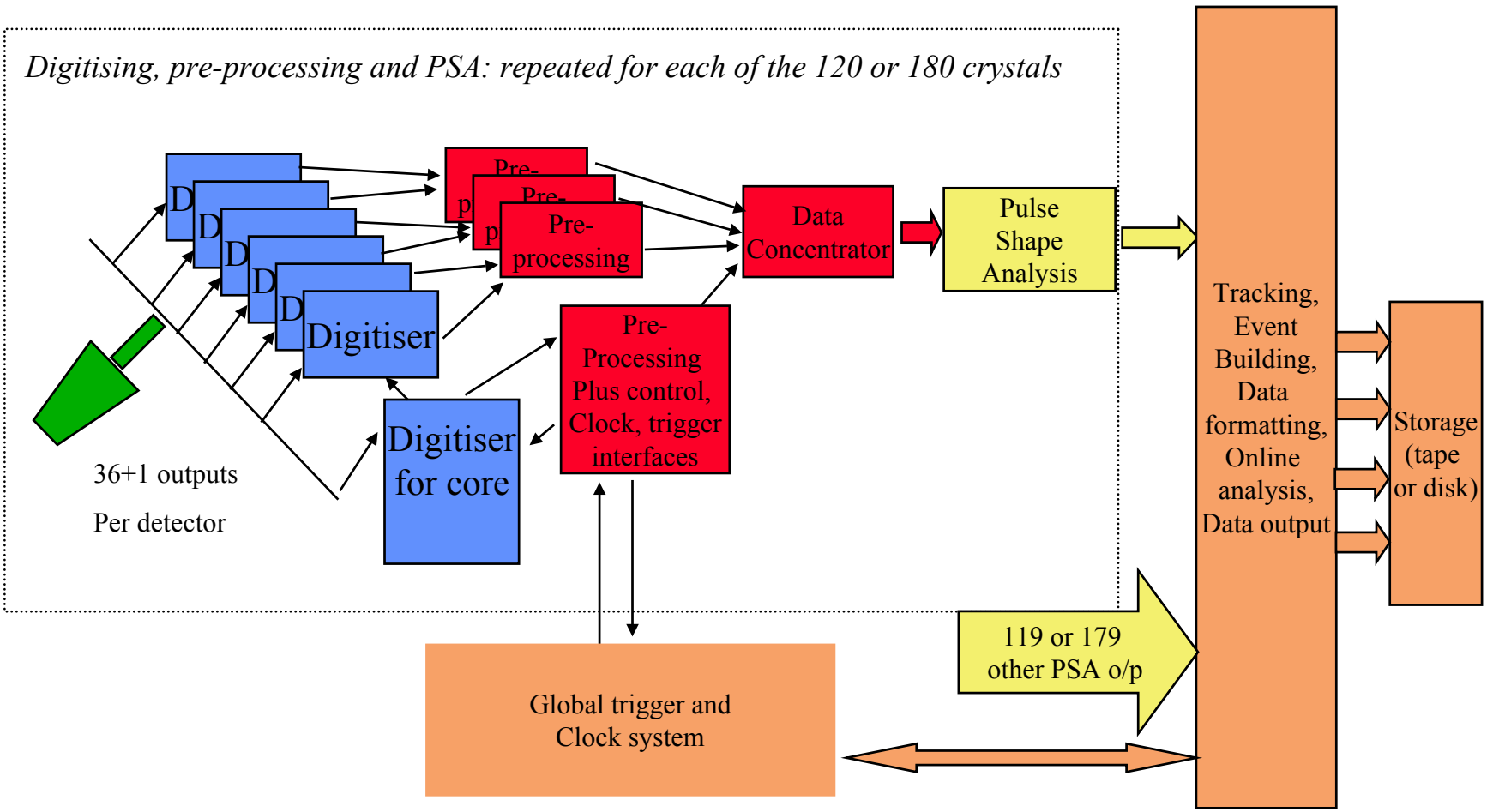
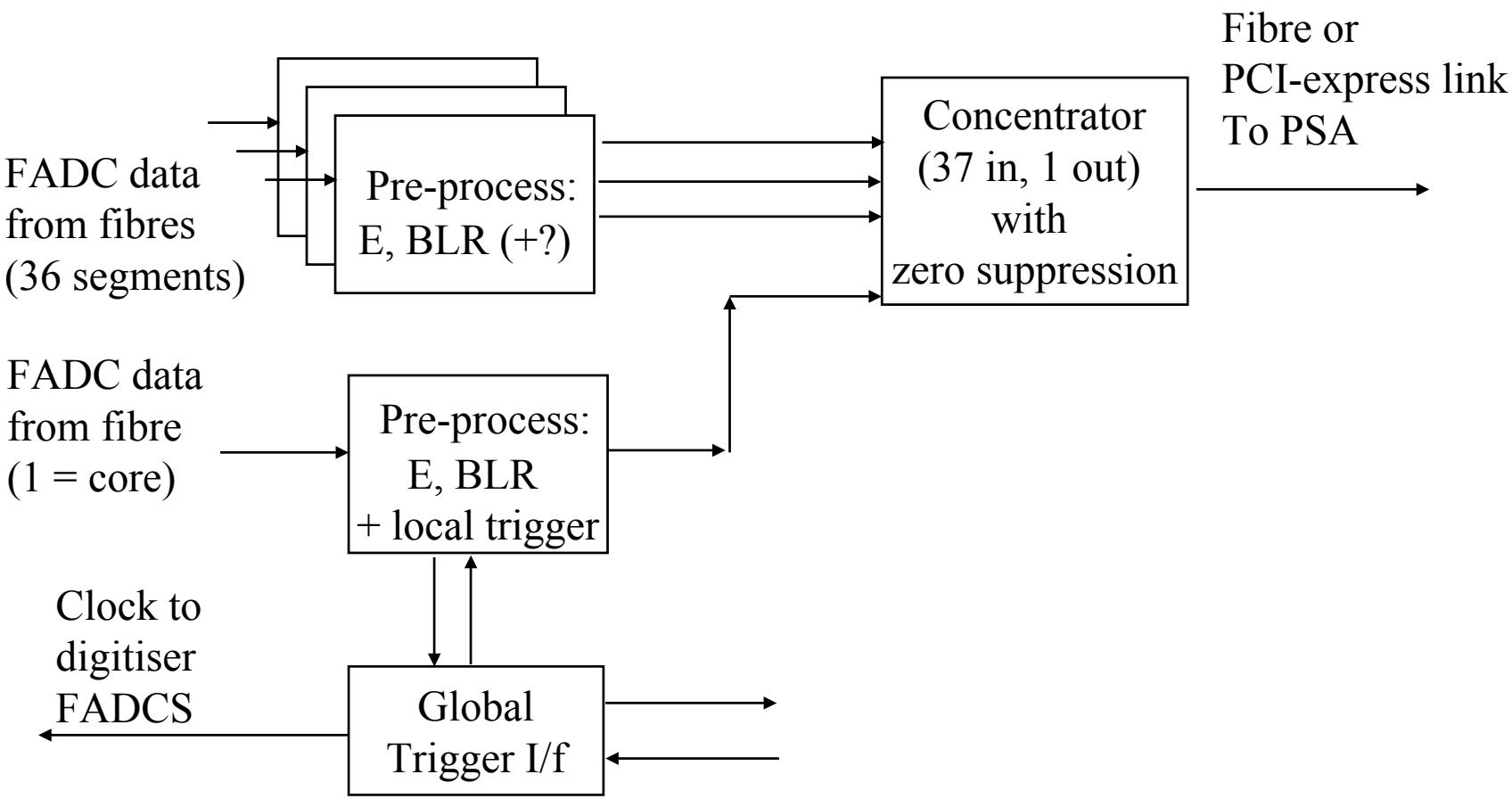
AGATA Pre-processing

Report for September 2003 AGATA week.

Schematic System Diagram June 2003



Pre-processing and concentrator



Pre-processing and data concentrator

- Fibre receiver and deserialiser per input
- Calculates energy (if not done already)
- Digital Baseline Restorer (with digitiser)
- Concentrates data from all 36 segments+core.
- Performs zero suppression
- Associates timestamp with the traces
- Perhaps do other simple algorithms if they save time in the PSA stage by reducing iterations and are significantly faster in hardware than PSA software.

Pre-processing group

Membership of the pre-processing team is still open.

Up to now the work has been done by these people:

- Marco Bellato
- Pierre Edelbruck
- Xavier Grave
- Roberto Isocrate
- Ian Lazarus
- Sebastien Lhenoret
- Denis Linget
- Christophe Oziol

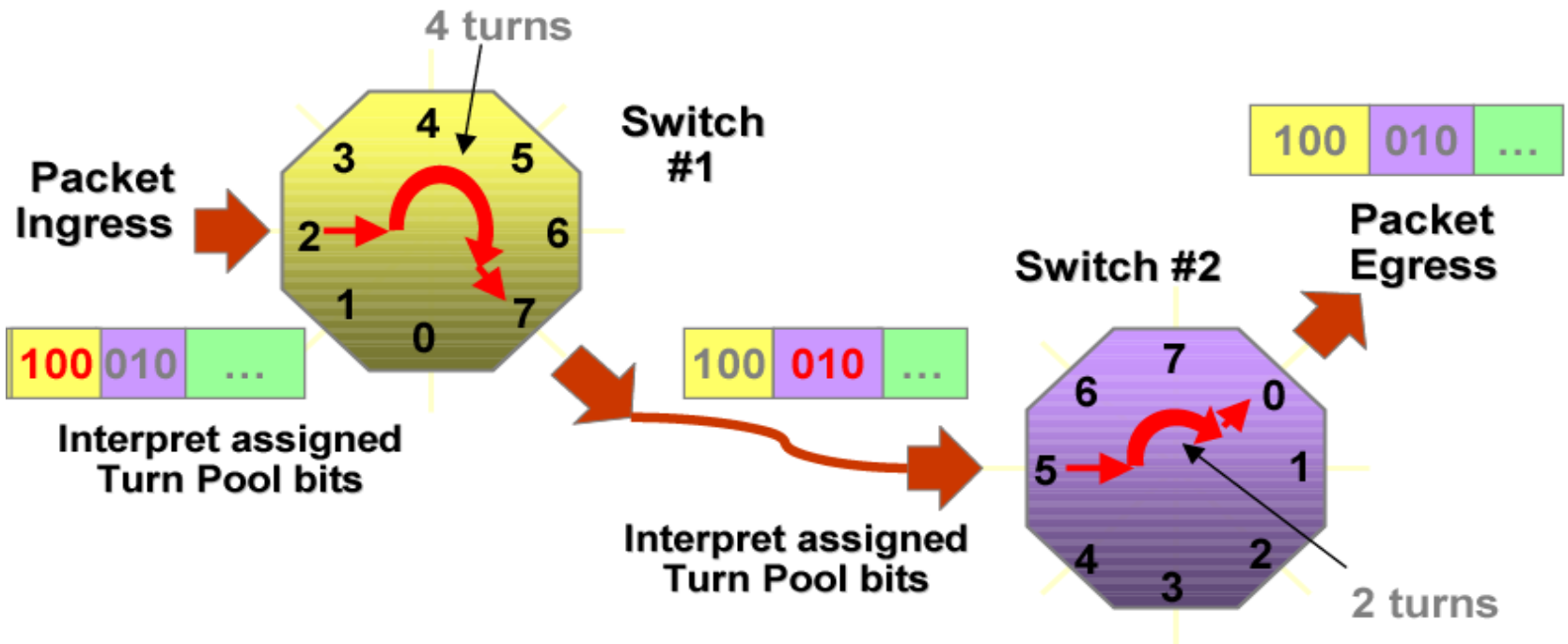
Pre-processing design constraints

- Main constraint is time- so we must maximise re-useability (also reduces cost).
- Another constraint is the time taken for the design and layout of high speed PCBs, especially the GHz parts near the SERDES.
- Need good i/o bandwidth and would like to exploit the features of the new advanced switching backplanes, but these are not quite ready yet.

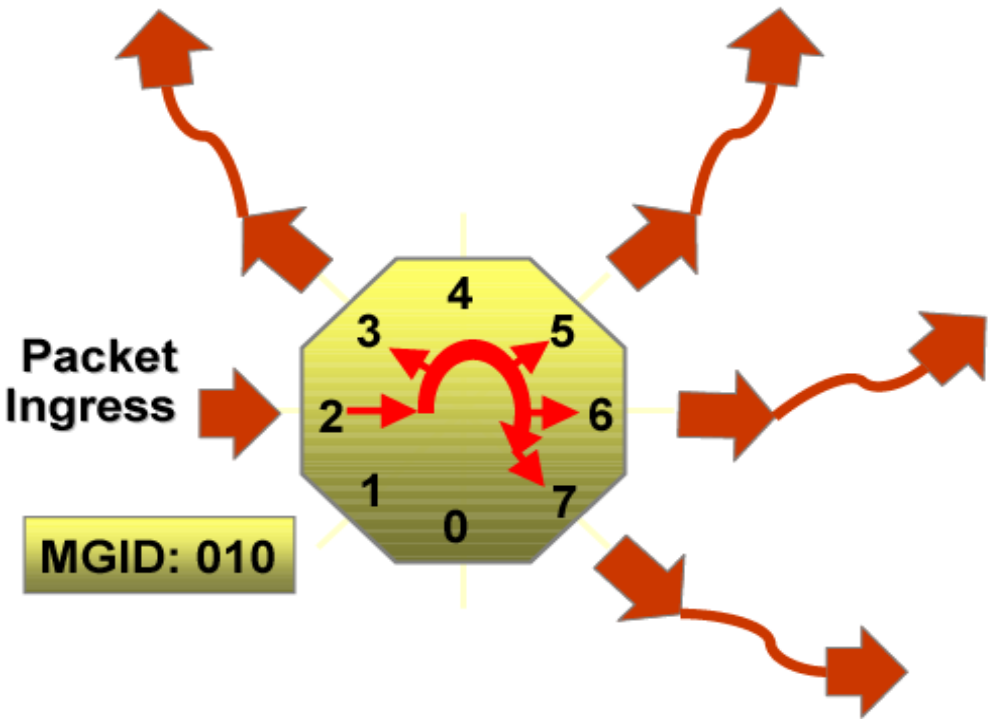
Pre-processing plan of action

- The proposal we present here is modular.
- Based on CMC mezzanines which can be mounted on different carriers- initially CPCI; later PCI Express (AS)/ATCA (or anything else)
- The high speed input design is all re-used.
- The carrier design can be partially re-used when we move to an advanced switching system.

Why PCI Express (AS)? No route table needed



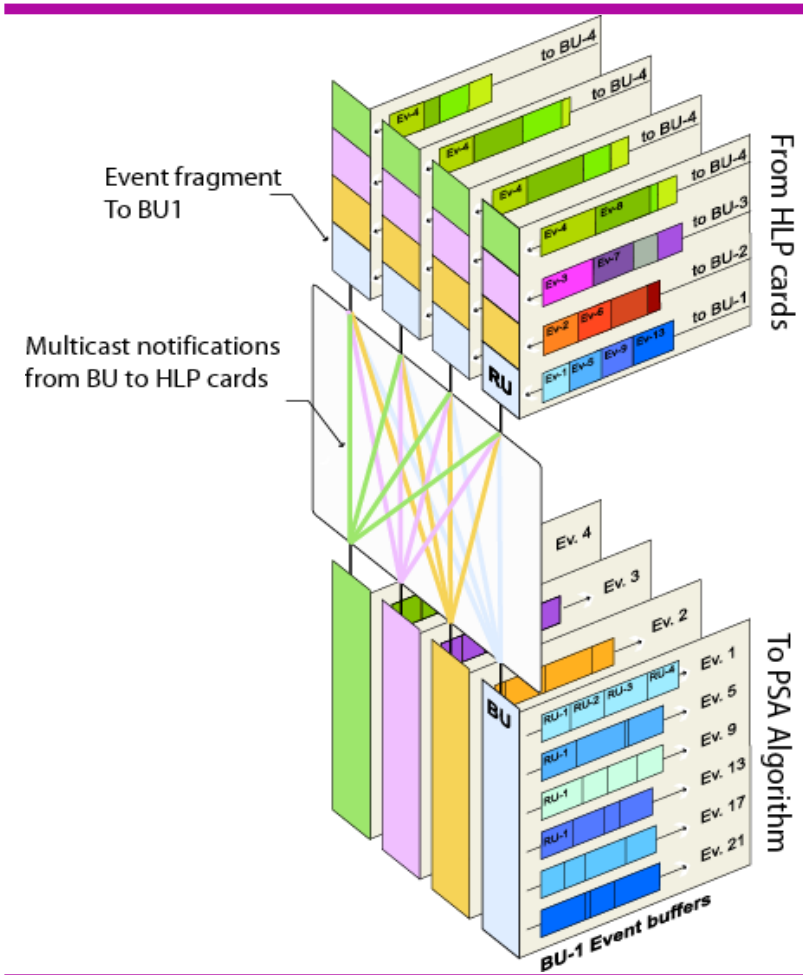
Why PCI Express (AS)? Broadcast/multicast



Interpret assigned multicast ID (Compare in Multicast Table)

MGID	OUTPUT PORT 0	1	2	3	4	5	6	7
000	0	0	0	1	1	0	0	0
001	0	1	0	0	1	1	0	0
010	0	0	0	1	0	1	1	1

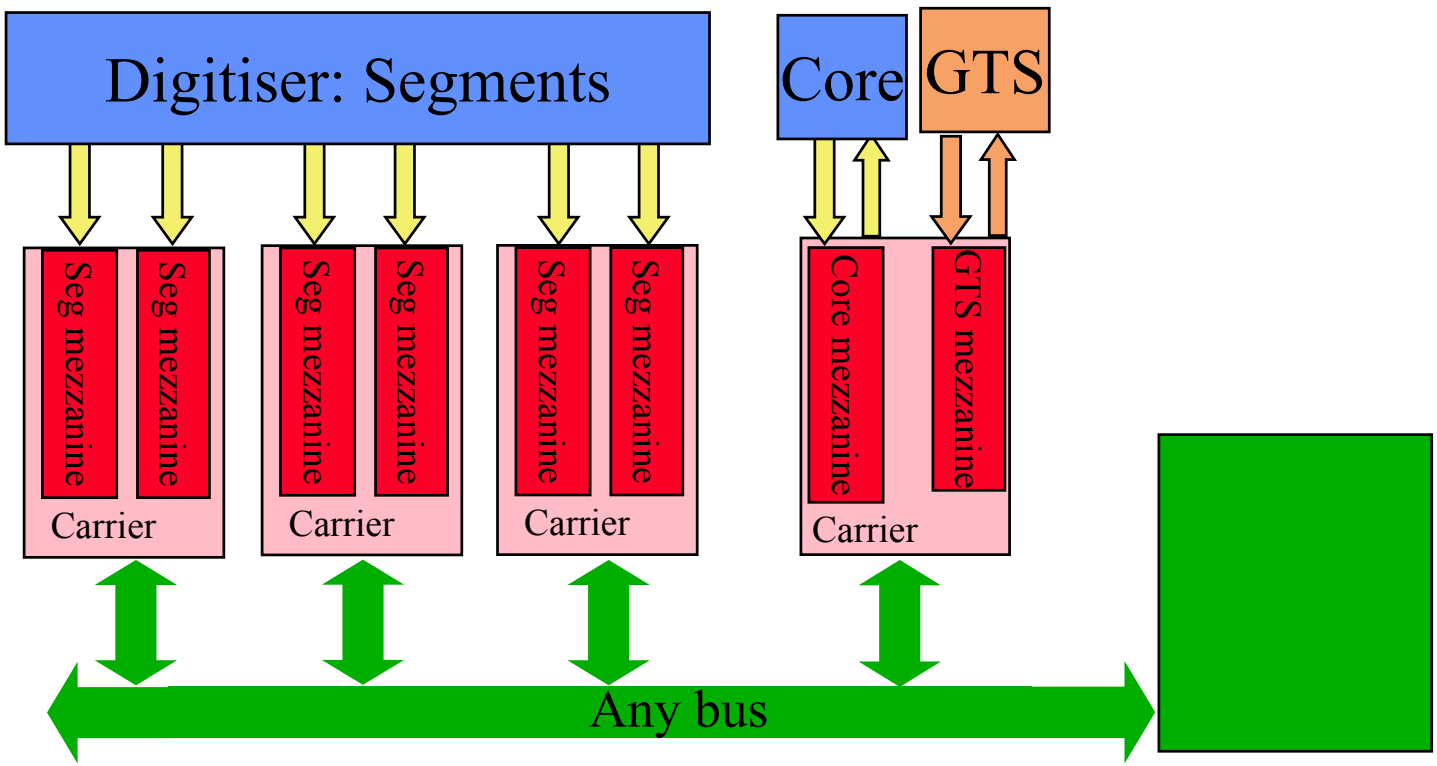
Distributed event building in ATCA



Pre-processing "pushes" data to PSA.

Multicasts from PSA processors request the next event from pre-processing when available

Pre processing for a single crystal



Segment Mezzanine

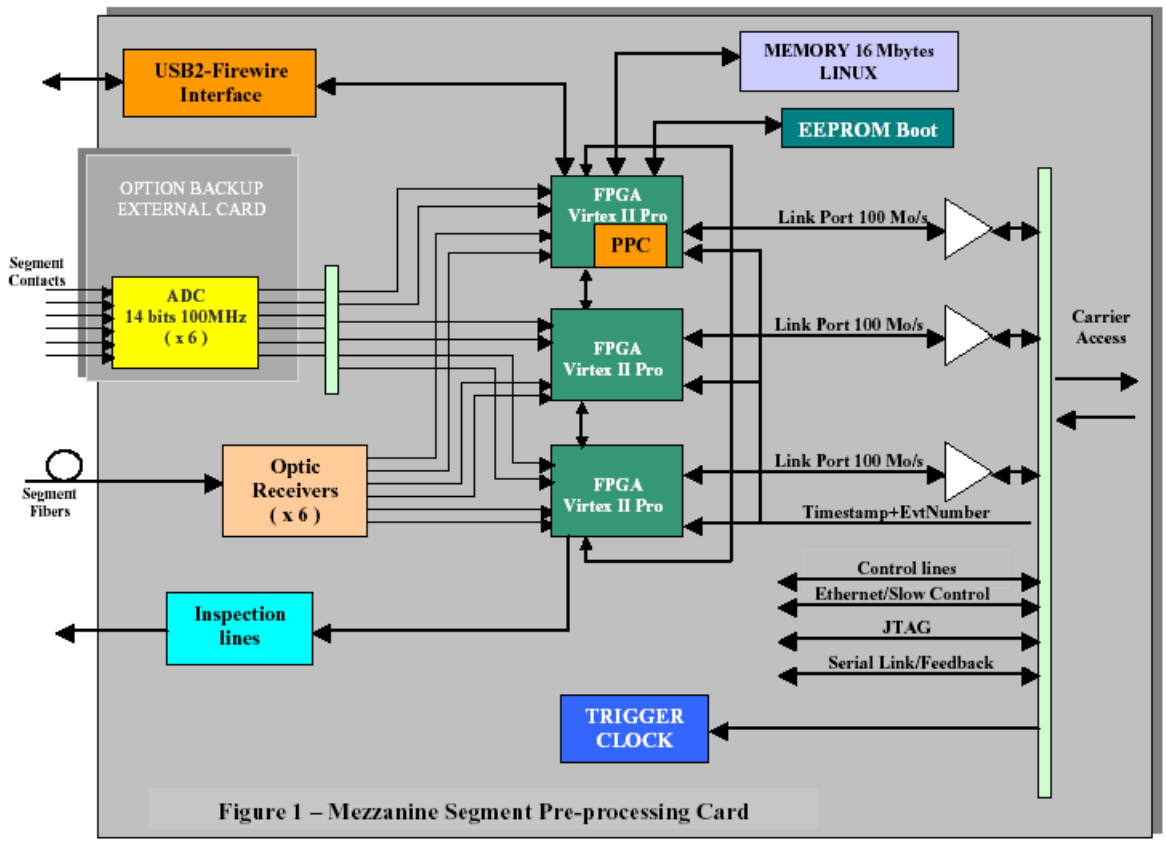


Figure 1 – Mezzanine Segment Pre-processing Card

Core Mezzanine

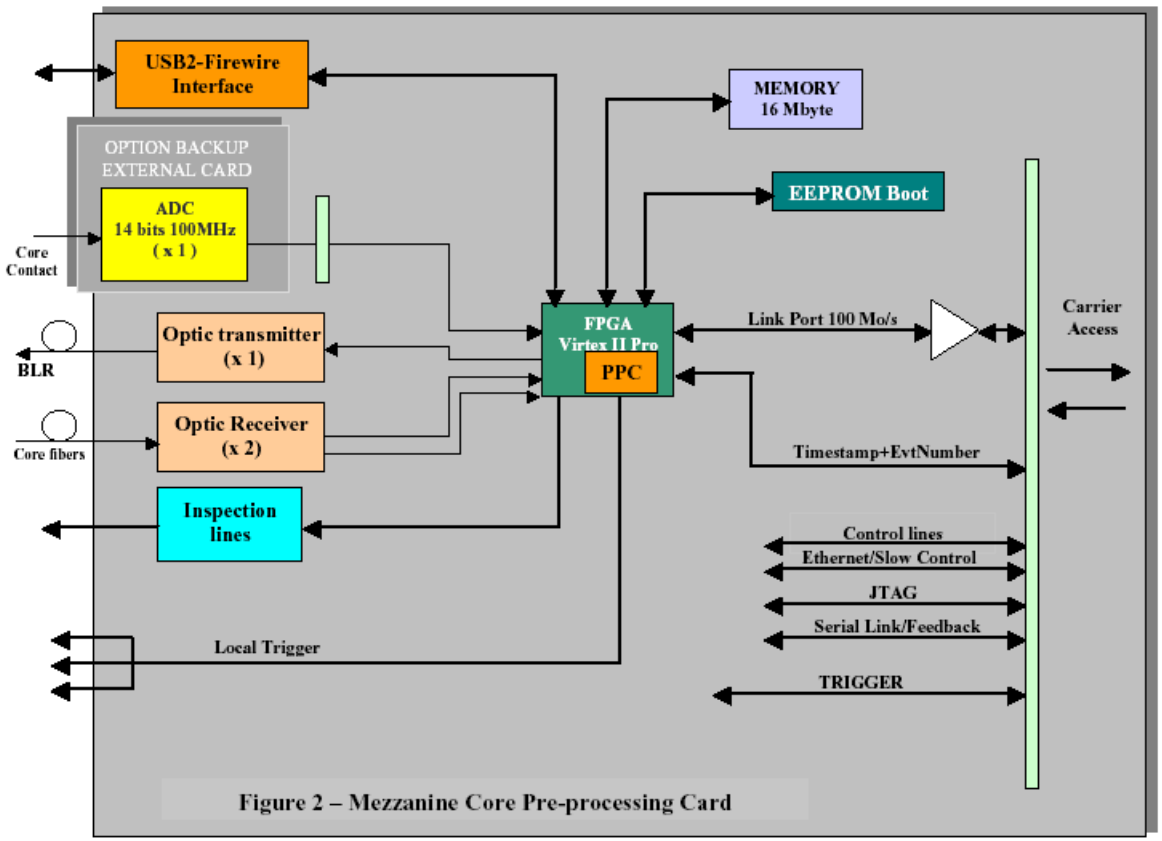


Figure 2 – Mezzanine Core Pre-processing Card

GTS Mezzanine

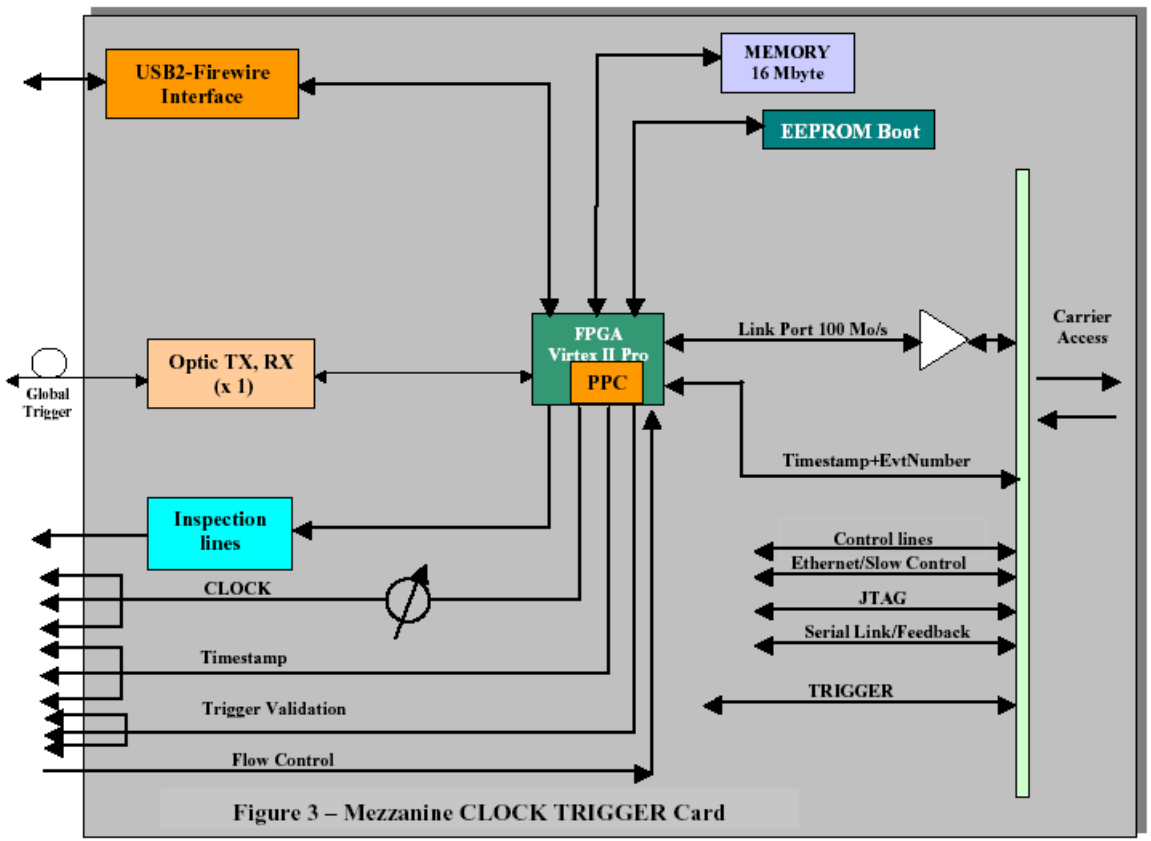
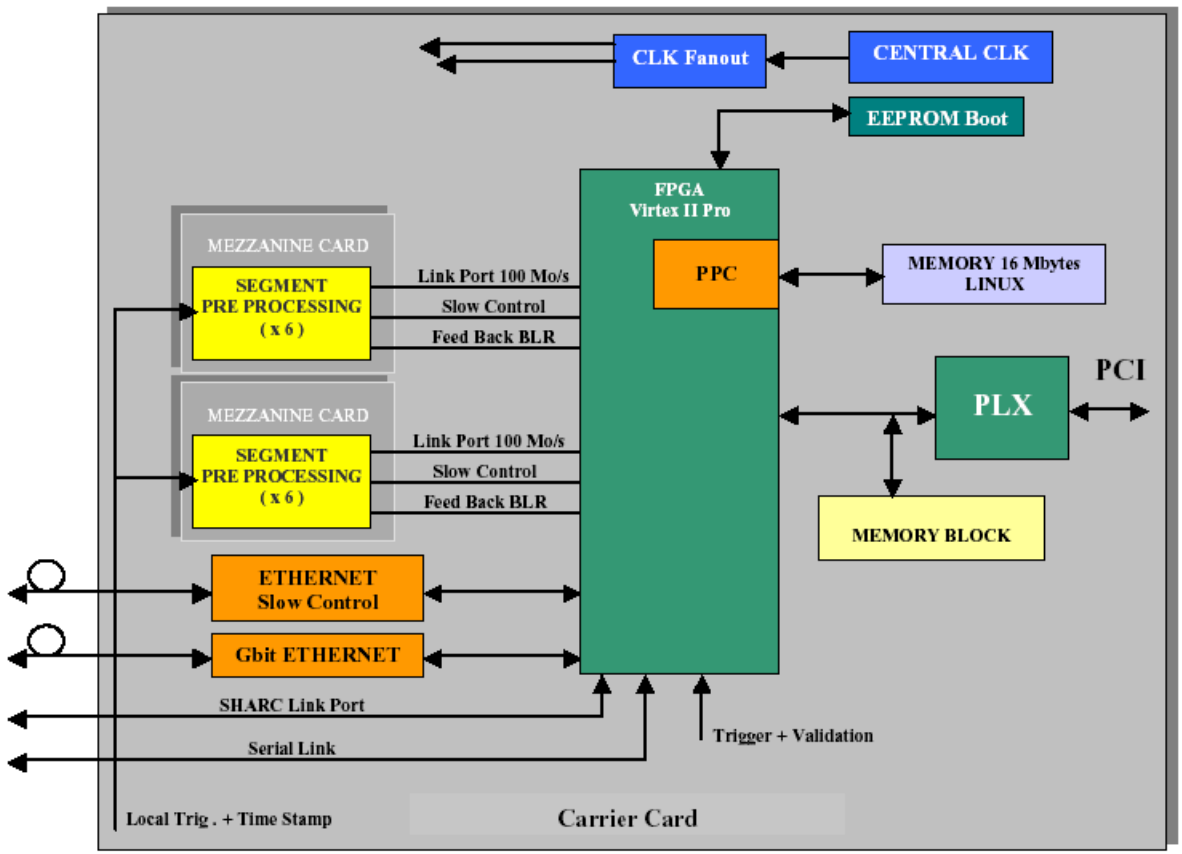
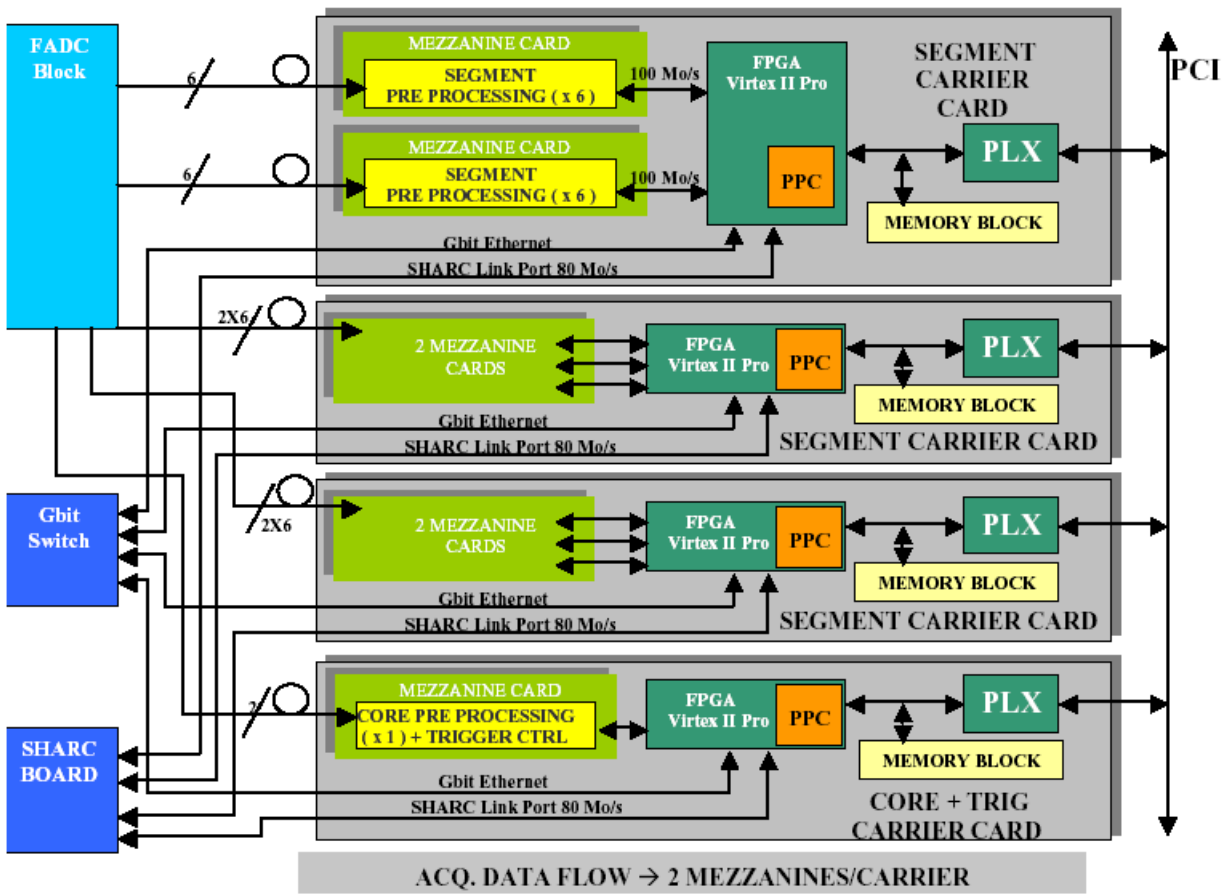


Figure 3 – Mezzanine CLOCK TRIGGER Card

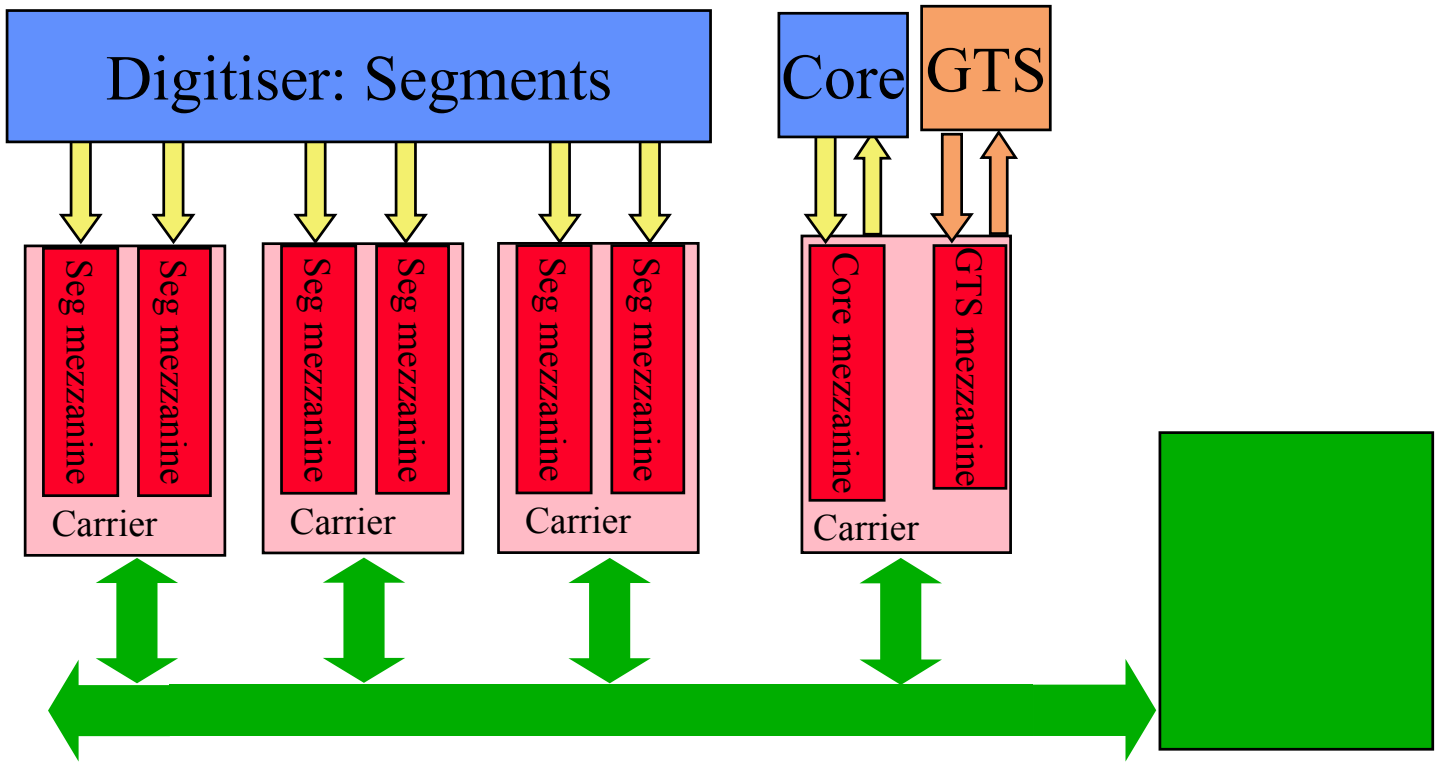
Carrier Card



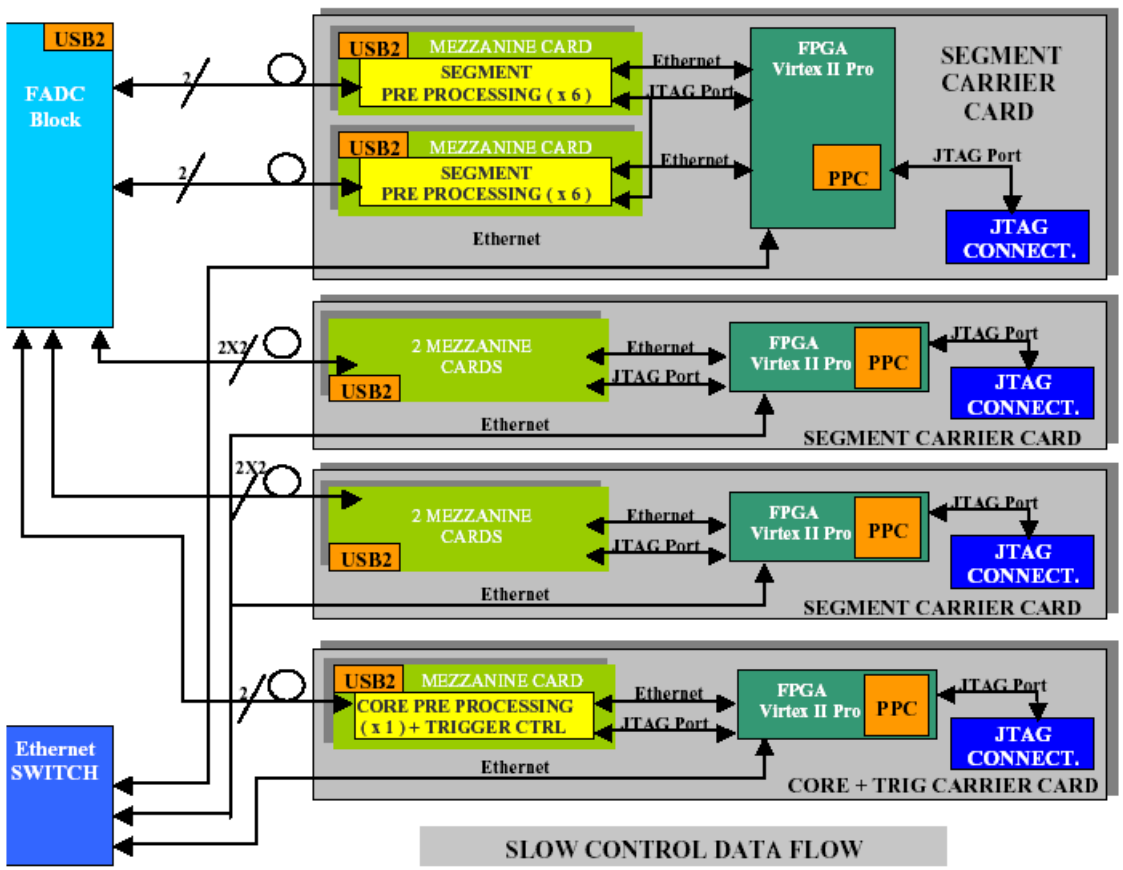
Pre-processing for a single crystal (detail)



Pre processing for a single crystal (generic)



Slow Control



USB or Firewire in the lab For standalone testing.

Ethernet externally and internally between FPGAs for reading and writing all parameters

Digitiser read/write access comes via the pre-processing down fibres

JTAG for test and FPGA loading

Global Clock and Trigger interface

- Pre-processing has a dedicated GTS mezzanine.
- Receives and distributes system clock for pre-processing and its associated digitiser
- Carries time-sensitive control (stop/go…)
- Core pre-processing contains trigger logic-generates local trigger to all mezzanines
- GTS mezzanine confirms readout by trigger validation (locally generated or from GTS)

Approximate costing for 1 crystal prototype

- 4 carriers @ €1500 = €6000
- 6 seg mezz @ €2000 = €12000
- 1 core mezz @ €2000 = €2000
- 1 GTS mezz @ €2000 = €2000
- 1 CPCI system @ €6000 = €6000
- **TOTAL = €28000**

Estimated manpower for 1 crystal prototype

- Digitizer mezzanine- h/w 0.75SY
- Digitizer mezzanine- FPGA 2x 0.75SY
- CPCI carrier- hardware 0.75SY
- CPCI carrier FPGA 0.75SY
- CPCI carrier linux software 1.0SY
- GTS mezzanine- h/w 0.75SY
- GTS mezzanine- FPGA 0.5SY
- Change carrier to ATCA 0.5SY
- PCI Express research 0.5SY
- **TOTAL 7SY**

Estimated manpower for 1 crystal prototype

• Digitizer mezzanine- h/w	CSNSM Orsay
• Digitizer mezzanine- FPGA	CSNSM Orsay
• CPCI carrier- hardware	IPN Orsay
• CPCI carrier FPGA	Daresbury
• CPCI carrier linux software	IPN Orsay
• GTS mezzanine- h/w	Padova
• GTS mezzanine- FPGA	Padova
• Change carrier to ATCA	IPNO/DL??
• PCI Express research	??
• TOTAL	7SY *(9/10 people)*

Timescale

- Produce outline specs by 15th Sept 2003
- Detailed specs and discussion Q4 2003
- Prototype design and build Q1-Q4 2004
- Prototype test and rework Q1-Q2 2005
- Production Q3 2005 to Q3 2006
- Part system commissioning Q3 2006
- Full system commissioning Q4 2006
- Demonstrator ready for physics 1st Jan 2007

Maintenance and support

Although designed for reliability, problems will occur- what happens then?

1. *Built in test paths (JTAG)*
2. *Self test/diagnosis using carrier's PPCs*
3. *Deliverables must include full documentation and test programs, not just the hardware/software.*
4. *Host lab support people- involve them all through project- build knowledge, ownership*
5. *Repairs- commercial contract? Employ someone to maintain & repair electronics?*

Commercial Options

- **Commercial in confidence**
- The following pages describe systems which are new developments by three commercial companies.
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