

FPGA1 Buffers management and JTAG switch I2C data format

I2C STREAM FORMAT

1st Byte



2nd Byte



3rd Byte

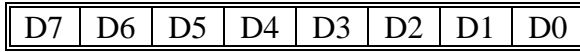


MEMORY SPACE LAYOUT

Subaddress	Description	Comment
\$00	PICMG_ADDRESS	
\$01	CMC1_REGISTER	
\$02	CMC2_REGISTER	
\$03	CMC3_REGISTER	
\$04	CMC4_REGISTER	
\$05	FPGA0_REGISTER	
\$06	FPGA1_REGISTER	
\$07	SWITCH0_REGISTER	
\$08	SWITCH1_REGISTER	
\$09	FAB_CH1_RX	MGT109A
\$0A	FAB_CH1_TX	MGT109A
\$0B	FAB_CH2_RX	MGT109B
\$0C	FAB_CH2_TX	MGT109B
\$0D	FAB_CH3_RX	MGT106B
\$0E	FAB_CH3_TX	MGT106B
\$0F	FAB_CH4_RX	MGT106A
\$10	FAB_CH4_TX	MGT106A
\$11	FAB_CH5_RX	MGT105B
\$12	FAB_CH5_TX	MGT105B
\$13	FAB_CH6_RX	MGT105A
\$14	FAB_CH6_TX	MGT105A
\$15	FAB_CH7_RX	MGT103B
\$16	FAB_CH7_TX	MGT103B
\$17	FAB_CH8_RX	MGT103A
\$18	FAB_CH8_TX	MGT103A
\$19	FAB_CH9_RX	MGT102B
\$1A	FAB_CH9_TX	MGT102B
\$1B	FAB_CH10_RX	MGT102A
\$1C	FAB_CH10_TX	MGT102A
\$1D	FAB_CH11_RX	MGT101B
\$1E	FAB_CH11_TX	MGT101B
\$1F	FAB_CH12_RX	MGT101A
\$20	FAB_CH12_TX	MGT101A
\$21	FAB_CH13_RX	MGT114A
\$22	FAB_CH13_TX	MGT114A
\$23	FAB_CH14_RX	MGT114B
\$24	FAB_CH14_TX	MGT114B
\$25	FAB_CH15_RX	MGT113A
\$26	FAB_CH15_TX	MGT113A
\$27 to \$3F	Unused	

SUBADDRESS \$07

SWITCH0_REGISTER



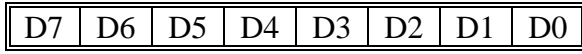
+----- SWITCH0_REGISTER -----+

Status / Configuration of clock and syncs switches

D0: R/W	GTS_LOC_SEL0	<i>Clock source for TCLK OUT</i>	0 → GTS 1 → Local Oscillator
D1: R/W	GTS_LOC_SEL1	<i>Clock source for PLL SW</i>	0 → GTS 1 → Local Oscillator
D2: R/W	TCLK_INT_SEL0	<i>Clock source for PLL0</i>	0 → PLL SW 1 → TCLK IN
D3: R/W	TCLK_INT_SEL1	<i>Clock source for INSP0</i>	0 → PLL SW 1 → TCLK IN
D4: R/W	MGT_GTS_LOC_SEL0	<i>Clock source for INSP1</i>	0 → GTS (100MHz) 1 → Local XTAL
D5: R/W	MGT_GTS_LOC_SEL1	<i>Base 100MHz PCI clock Source</i>	0 → GTS (100MHz) 1 → Local XTAL
D6: R/W	MGT_PCI_SEL0	<i>100MHz SFP clock Source</i>	0 → Base 100MHz (Local) 1 → SFP clock (Remote)
D7: R/W	MGT_PCI_SEL1	<i>100MHz PCI clock Source</i>	0 → Base 100MHz (Local) 1 → SFP clock (Remote)

SUBADDRESS \$08

SWITCH1_REGISTER



+----- SWITCH0_REGISTER -----+

Status / Configuration of clock and syncs switches

D0: R/W	SYNC_CHP_SEL	<i>Chipsync SYNC pattern source</i>	0 → TCLK IN 1 → Local
D1: R/W	SYNC_PLL_SEL	<i>PLL SYNC signal source</i>	0 → GTS (local) 1 → TCLK IN
D2: R/W	SYNC_ADC_SEL0	<i>ADC SYNC pattern source</i>	0 → GTS (local) 1 → TCLK IN
D3: R/W	SYNC_ADC_SEL1	<i>TCLK ADC SYNC pattern source</i>	0 → GTS (local) 1 → TCLK IN
D4: R/W	ON_SFP_CLOCK	<i>SFP Clock on/off command</i>	0 → OFF 1 → POWER ON
D5: R/W	ON_SFP_LANES	<i>SFP Data on/off command</i>	0 → OFF 1 → POWER ON
D[7..6] : Read/Write Unused			

