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FPGA1 Buffers management and JTAG switch I2C data format

I2C STREAM FORMAT

1st Byte

							R/W

+----------------ADDRESS----------------+

2nd Byte

							_/_ _

+------------SUB ADDRESS---------------+

3rd Byte

							_/_ _

+------------ ---- DATA ---------------------+

MEMORY SPACE LAYOUT

Subaddress	Description	Comment
$00	PICMG_ADDRESS	
$01	CMC1_REGISTER	
$02	CMC2_REGISTER	
$03	CMC3_REGISTER	
$04	CMC4_REGISTER	
$05	FPGA0_REGISTER	
$06	FPGA1_REGISTER	
$07	SWITCH0_REGISTER	
$08	SWITCH1_REGISTER	
$09	FAB_CH1_RX	MGT109A
$0A	FAB_CH1_TX	MGT109A
$0B	FAB_CH2_RX	MGT109B
$0C	FAB_CH2_TX	MGT109B
$0D	FAB_CH3_RX	MGT106B
$0E	FAB_CH3_TX	MGT106B
$0F	FAB_CH4_RX	MGT106A
$10	FAB_CH4_TX	MGT106A
$11	FAB_CH5_RX	MGT105B
$12	FAB_CH5_TX	MGT105B
$13	FAB_CH6_RX	MGT105A
$14	FAB_CH6_TX	MGT105A
$15	FAB_CH7_RX	MGT103B
$16	FAB_CH7_TX	MGT103B
$17	FAB_CH8_RX	MGT103A
$18	FAB_CH8_TX	MGT103A
$19	FAB_CH9_RX	MGT102B
$1A	FAB_CH9_TX	MGT102B
$1B	FAB_CH10_RX	MGT102A
$1C	FAB_CH10_TX	MGT102A
$1D	FAB_CH11_RX	MGT101B
$1E	FAB_CH11_TX	MGT101B
$1F	FAB_CH12_RX	MGT101A
$20	FAB_CH12_TX	MGT101A
$21	FAB_CH13_RX	MGT114A
$22	FAB_CH13_TX	MGT114A
$23	FAB_CH14_RX	MGT114B
$24	FAB_CH14_TX	MGT114B
$25	FAB_CH15_RX	MGT113A
$26	FAB_CH15_TX	MGT113A
$27 to $3F	Unused	

REGISTERS DESCRIPTION

SUBADDRESS $00

PICMG ADDRESS

D7	D6	D5	D4	D3	D2	D1	D0

+--------- PICMG ADDRESS-------------+

Read only

PICMG ADDRESS : Indicate the slot were the card is inserted

SUBADDRESS $01 to $04

CMC_REGISTER

Subaddress $01 → CMC1_REGISTER (Top)
$02 → CMC2_REGISTER
$03 → CMC3_REGISTER
$04 → CMC4_REGISTER (Bottom)

D7	D6	D5	D4	D3	D2	D1	D0

+--------- CMC_REGISTER-------------+

Status / Configuration of CMC slot :

D[1..0] : *Read only* *CMC conf* :
00 → Not installed
01 → GTS
10 → Core
11 → Segment

D[2..3] : *Read/Write* *Data deskew* [0 to 3]

D[4] : *Read Only* *Fpga done signal*

D[6..5] : *Read/Write* *FPGA Code selection* [0 to 3]

D[7] : *Read/Write* *JTAG switch bypass*
0 → Inserted (*)
1 → Bypassed

(*) If CMC Conf is 00 (Not installed) The Jtag is bypassed by default

SUBADDRESS $05 to $06

FPGA_REGISTER

Subaddress $05 → FPGA0_REGISTER (Main Virtex4 FX60/100)
$06 → FPGA1_REGISTER (Trigger Virtex4 LX25)

D7	D6	D5	D4	D3	D2	D1	D0

+--------- FPGA_REGISTER-------------+

Status / Configuration of FPGAs :

D[2..0] : *Read/Write* *Unused*

D3 : *Read/Write* *Enable code selection* 0 → Disable
1 → Enable

D4 : *Read Only* *Fpga done signal*

D[6..5] : *Read/Write* *FPGA Code selection [0 to 3]*

D[7] : *Read/Write* *JTAG switch bypass* 0 → Inserted
1 → Bypassed

SUBADDRESS $07

SWITCH0_REGISTER

D7	D6	D5	D4	D3	D2	D1	D0

+------- SWITCH0_REGISTER ---------+

Status / Configuration of clock and syncs switches

D0: R/W	GTS_LOC_SEL0 *Clock source for TCLK OUT*	0→ GTS 1→ Local Oscillator
D1: R/W	GTS_LOC_SEL1 *Clock source for PLL SW*	0→ GTS 1→ Local Oscillator
D2: R/W	TCLK_INT_ SEL0 *Clock source for PLL0*	0→ PLL SW 1→ TCLK IN
D3: R/W	TCLK_INT_ SEL1 *Clock source for INSP0*	0→ PLL SW 1→ TCLK IN
D4: R/W	MGT_GTS_LOC_SEL0 *Clock source for INSP1*	0→ GTS (100MHz) 1→ Local XTAL
D5: R/W	MGT_GTS_LOC_SEL1 *Base 100MHz PCI clock Source*	0→ GTS (100MHz) 1→ Local XTAL
D6: R/W	MGT_PCI_ SEL0 *100MHz SFP clock Source*	0→ Base 100MHz (Local) 1→ SFP clock (Remote)
D7: R/W	MGT_PCI_ SEL1 *100MHz PCI clock Source*	0→ Base 100MHz (Local) 1→ SFP clock (Remote)

SUBADDRESS $08

SWITCH1_REGISTER

D7	D6	D5	D4	D3	D2	D1	D0

+------- SWITCH0_REGISTER ---------+

Status / Configuration of clock and syncs switches

D0: R/W SYNC_CHP_SEL *Chipsync SYNC pattern source* 0→ TCLK IN
1→ Local

D1: R/W SYNC_PLL_SEL *PLL SYNC signal source* 0→ GTS (local)
1→ TCLK IN

D2: R/W SYNC_ADC_SEL0 *ADC SYNC pattern source* 0→ GTS (local)
1→ TCLK IN

D3: R/W SYNC_ADC_SEL1 *TCLK ADC SYNC pattern source* 0→ GTS (local)
1→ TCLK IN

D4: R/W ON_SFP_CLOCK *SFP Clock on/off command* 0→ OFF
1→ POWER ON

D5: R/W ON_SFP_LANES *SFP Data on/off command* 0→ OFF
1→ POWER ON

D[7..6] : Read/Write Unused

SUBADDRESS $09 to $38

GIGABIT_BUFFER_REGISTER

D7	D6	D5	D4	D3	D2	D1	D0

+--- GIGABIT_BUFFER_REGISTER ---+

Configuration of PERICOM Gigabit repeaters

D[1..0]	: *Read/Write*	*Equalization*	00 → no equalization 01 → 0 : 2.5dB 10 → 1.5 : 4.5dB 11 → 4.5 : 6.5dB
D2	: *Read/Write*	*Swing Sel*	0 → 1.0x 1 → 1.2x
D3	: *Read/Write*	*De-emphasis*	0 → 0 dB 1 → -3.5dB
D4	: *Read/Write*	*Chl Enable*	0 → Disable 1 → Enable
D[7..5]	: *Read/Write*	*Unused*	

SUBADDRESS $39 to $63

Read/Write : Unused .